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Low – Power TSPC Flip-Flop with Auto-Gated Clock Gating, Power Gating and Redundant-Transition Suppression

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ABSTRACT

An advanced low-power True Single Phase Clock (TSPC) flip-flop design leveraging a synergistic integration of three power-saving techniques: auto-gated clock gating, power gating, and redundant-transition suppression. The proposed architecture targets both dynamic and leakage power reduction in sequential circuits without sacrificing speed or timing integrity. Auto-gated clock gating dynamically disables the clock signal when input data remains stable, eliminating unnecessary switching activity. Power gating is employed to disconnect the power supply to idle flip-flop stages during prolonged inactivity, significantly reducing static leakage current. Additionally, redundant-transition suppression logic prevents internal node toggling in response to non-transitioning inputs, further minimizing dynamic power dissipation. These techniques are seamlessly embedded within the TSPC structure, preserving its inherent advantages such as single-phase clock operation and high-speed performance. The design is implemented and verified through post-layout simulations in a standard CMOS technology, demonstrating substantial improvements in energy efficiency compared to conventional TSPC and other existing low-power flip-flop designs. Results indicate significant reductions in both active and standby power consumption, achieving superior energy-delay product metrics. The proposed flip-flop is particularly well-suited for high-performance digital systems operating under stringent energy constraints, such as portable and battery-powered devices. By intelligently managing clock and power resources while maintaining robust functionality, this design offers a practical and scalable solution for next-generation energy-efficient integrated circuits.

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Keywords: TSPC Flip-Flop; Low-Power Design; Clock Gating; Power Gating; Redundant-Transition Suppression; Dynamic Power Reduction; Energy-Efficient Circuits; CMOS Design

1. Introduction

In modern digital integrated circuit design, power efficiency has become a critical concern, especially with the increasing demand for portable and battery-operated devices. Among the key contributors to dynamic power consumption in synchronous systems are clocked sequential elements such as flip-flops, which are used extensively in data storage and synchronization. Traditional flip-flop architectures often suffer from high power dissipation due to continuous clock switching and unnecessary internal node transitions, even when data remains unchanged.

To address these challenges, advanced low-power flip-flop designs have been developed, integrating multiple power-saving techniques. One such approach is the True Single-Phase Clock (TSPC) flip-flop, known for its simplicity and reduced transistor count. However, even TSPC flip-flops can benefit from further optimization. This has led to the development of enhanced TSPC-based flip-flops incorporating auto-gated clock gating, power gating, and redundant-transition suppression mechanisms. Auto-gated clock gating dynamically disables the clock signal to the flip-flop when there is no change in input data, thereby minimizing switching activity and reducing dynamic power. Power gating complements this by cutting off the supply voltage to idle circuit blocks, significantly lowering leakage power during inactive periods. Additionally, redundant-transition suppression prevents unnecessary internal node toggling when the input data is identical to the stored value, further reducing both dynamic and short-circuit power[1].

By combining these three techniques, the proposed low-power TSPC flip-flop achieves substantial energy savings without compromising performance or reliability, making it highly suitable for energy-constrained and high-density digital systems. This integration represents a holistic approach to minimizing both active and standby power consumption in modern VLSI designs.

2. Survey of Low-Power Design Objectives in Sequential Circuits

In modern VLSI design, minimizing power consumption is a primary objective, especially for portable, wearable, and IoT devices where energy efficiency directly impacts battery life and thermal management. Sequential circuits, particularly flip-flops, contribute significantly to a system's total power budget due to their continuous clock-driven switching activity.

The main goals of low-power design in flip-flops include Minimizing leakage (static) power, which becomes dominant at smaller technology nodes (e to sub-45nm), even when the circuit is idle. Preserving performance, ensuring that power optimization does not compromise speed or timing reliability. Maintaining area efficiency, avoiding excessive transistor count or complex control logic that could offset power savings.

To achieve these objectives, several techniques have been widely adopted to these strategies are often combined in advanced flip-flop designs like the True Single-Phase Clock (TSPC) architecture, which offers simplicity, speed, and compatibility with deep-submicron processes. Recent research focuses on integrating multiple such techniques synergistically to maximize energy efficiency without degrading circuit robustness. this work builds upon these established principles by proposing a TSPC-based flip-flop that integrates auto-gated clock gating, power gating, and redundant-transition suppression in a single, optimized structure achieving significant power reduction while maintaining functional integrity and timing performance[2].

3. Methodology

The primary goal of this design is to develop a high-performance, energy-efficient True Single-Phase Clock (TSPC) flip-flop tailored for use in power-sensitive digital systems. By integrating auto-gated clock gating, power gating, and redundant-transition suppression mechanisms,

the flip-flop aims to significantly reduce both dynamic and static power consumption without compromising speed or reliability.

3.1. TSPC Flip-Flop Base Architecture

The design begins with a standard True Single-Phase Clock (TSPC) flip-flop as the foundational building block due to its inherent advantages in speed and simplicity. The TSPC architecture employs a single-phase clock signal to control a cascaded structure of dynamic logic stages typically comprising a master latch and a slave latch each consisting of a clocked inverter pair and a static inverter. This configuration enables edge-triggered behavior using only one clock phase, eliminating the need for complementary clock signals and reducing clock distribution complexity.

Design and Analysis of SEU Hardened Latch for Low Power and High-Speed Applications. during the low phase of the clock, the master stage samples the input data, while the slave stage remains in hold mode. When the clock transitions high, the master stage isolates the input, and the slave stage evaluates and propagates the stored value to the output. This operation relies on careful timing and charge storage, allowing for fast switching with relatively low transistor count and minimal interconnect delay [3].

The TSPC flip-flop is particularly suitable for high-speed applications due to its dynamic nature and reduced propagation delay (**Figure 1**). While traditionally associated with higher leakage and dynamic power in idle states, its simple, compact layout provides an excellent platform for integrating advanced power-saving techniques such as auto-gated clock gating, fine-grained power gating, and redundant-transition suppression.

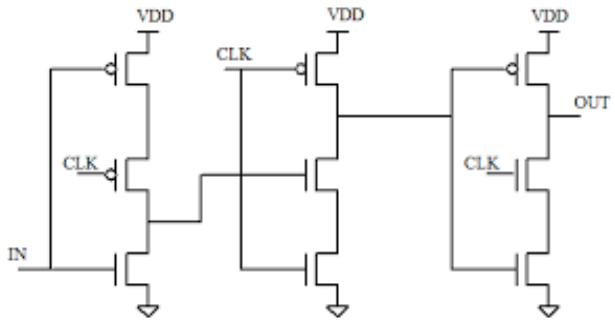

Figure 1. Schematic of the TSPC flip-flop base architecture.

3.2. Auto Gated Clock Gating

A novel design strategy for True Single-Phase Clock (TSPC) flip-flops, developed in response to the increasing need for energy-efficient digital circuits. The proposed architecture incorporates two key power-saving techniques: auto-gated clocking and power gating for suppressing redundant transitions. Together, these mechanisms effectively minimize unnecessary switching activity and leakage current, leading to substantial reductions in overall power consumption. Importantly, these improvements are achieved without compromising speed or reliability. This introductory section lays the foundation for a comprehensive examination of the design methodology, operational benefits, and performance characteristics of the enhanced TSPC flip-flop.

Clock Gating:

The auto Gated Flip-flop serves as the fundamental circuit in implementing the Low-Power Asynchronous Clock Gating (LACG) technique, essential for cutting down on digital circuit power consumption. As illustrated in **Figure 2** and supported by existing literature, the Auto-Gated Flip-Flop (AGFF) operates such that during the master latch becomes visible during the falling edge of the clock signal, allowing for data stability to be established before the subsequent rising edge. This ensures adherence to critical setup time requirements, crucial for reliable operation. Upon transitioning to an opaque state, the decision of An XOR gate determines if the condition of the slave latch should be altered or stay the same. If the slave latch remains unchanged, the clock pulse can be gated to conserve power. gated to conserve power or allowed to propagate as necessary for normal operation. However, despite its utility, the Auto-Gated Flip-Flop (AGFF) suffers from notable limitations. A 0.4V 0.5fJ/cycle TSPC Flip-Flop in 65nm LP CMOS with Retention Mode Controlled by Clock-Gating Cells [4].

Firstly, the gating mechanism primarily targets slave latches, neglecting other clock loads within the circuit. This leaves significant portions of the circuit unaltered and operating at full power, diminishing the overall effectiveness of power reduction strategies. Additionally, Flip-flops with timing restrictions that are located on critical paths present another challenge, as these flip-flops are typically excluded from gating to ensure timing integrity. This limitation not only hampers power-saving efforts but also introduces po-

tential performance bottlenecks in critical sections of the design.

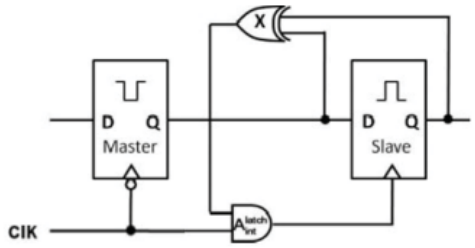

Figure 2. Block diagram of Auto gated clock gating.

Addressing these drawbacks is crucial for realizing the full potential of the LACG (Low-Power Asynchronous Clock Gating) technique in achieving low-power operation while maintaining optimal performance from the reference of block diagram of clock gating technique mentioned above, it is clear that it requires additional logic blocks of implementation for XOR and AND gate. In order to design these logic gate, here preferring Gated Diffusion Input (GDI) configuration which further helps in reduction of power consumption will approximately lesser utilization of MOSFET.

GDI [Gated Diffusion Input] Logic:

The number of transistors in a circuit significantly impacts its overall complexity, power consumption, and performance. In submicron CMOS technology, minimizing power and maximizing speed are key challenges, especially for low-power applications. Gated Diffusion Input (GDI) technology offers an effective solution by enabling simpler, more efficient circuit designs with reduced transistor count, lower power dissipation, and improved speed through optimized logic implementation (**Figure 3**, **Table 1**).

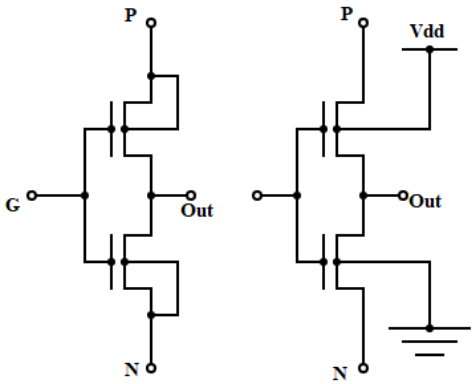

Figure 3. GDI structure.

Table 1. GDI function.

N	P	G	Output	Function
0	1	A	A’	NOT
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

3.3. Power Gating

In this design, power gating is integrated into the PMOS transistor to enhance energy efficiency (**Figure 4**). The technique involves disconnecting the power supply to idle circuit blocks using a sleep transistor, thereby significantly reducing leakage current during standby modes. By incorporating this method into the modified TSPC flip-flop, the circuit achieves lower static power consumption without affecting its operational integrity. This approach is particularly effective in deep-submicron CMOS technologies, where leakage power has become a major concern in low-power applications [5].

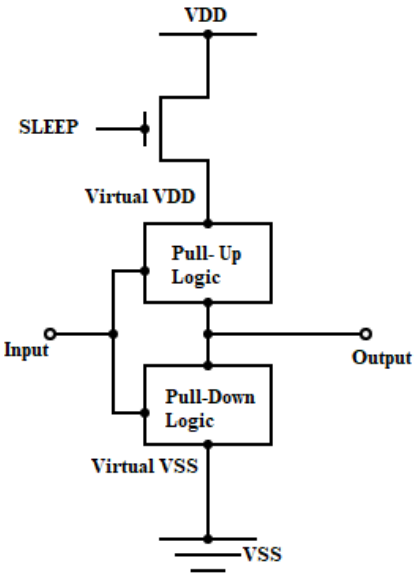

Figure 4. Block diagram of Power gating technique.

3.4. Redundant-Transition Suppression System

Redundant-transition suppression refers to the reduction of unnecessary internal state changes in a digital circuit when the input data matches the currently stored value (**Figure 5**). In sequential circuits like flip-flops, such transi-

tions do not result in a change in output but still cause switching activity in internal nodes, leading to wasteful dynamic and short-circuit power consumption. By detecting data stability and preventing internal node toggling during redundant transitions, significant power savings can be achieved. This technique is particularly effective in low-power VLSI design, where minimizing unnecessary switching activity enhances energy efficiency without compromising circuit performance or reliability. Integrating this method into flip-flop architectures helps reduce overall power dissipation, making it a valuable strategy for battery-operated and high-density digital systems[6].

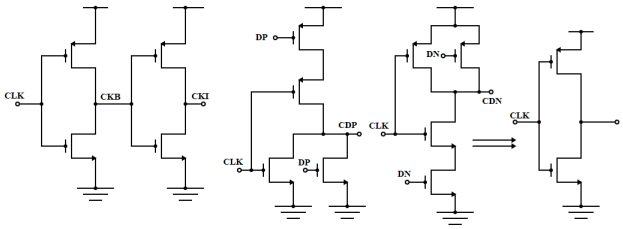

Figure 5. Schematic of the redundant transition FF.

The figure illustrates the design of a low-power TSPC (Transistor-Shared Pass-Gate Clocking) flip-flop with enhanced power-saving features. The leftmost circuit depicts the basic structure, where the clock signal (CLK) is buffered into complementary phases (Clock input and Clock bar). The middle section shows an intermediate stage that incorporates additional control signals (DP and DN) to enable dynamic power management.

Finally, the rightmost circuit demonstrates the optimized implementation, where the clock gating logic is simplified while maintaining functionality. This design approach reduces both dynamic and leakage power consumption by intelligently managing clock activity and minimizing redundant transitions, making it suitable for energy-efficient digital systems[7].

3.5. Single-Transition-Capture Double-Edge-Triggered (STCDET)

Capture of the term Single Transition STCDET refers to the dual-edge-triggered flip-flop. Comparing this specific flip-flop design to traditional ones, there are several advantages ones (**Figure 6**).

A dual-rail static edge-triggered latch. observation of a Single Capture STCDETs are double-edge-triggered flip-flops. Comparing this specific flip-flop design to traditional ones, there are several advantages STCDET flip-flops achieve higher data transfer rates than single-edge-triggered. Because STCDET flip-flops record data for a single clock cycle that includes both rising and falling clock edges, they effectively double the data transfer rate for quicker and more efficient data processing[8].

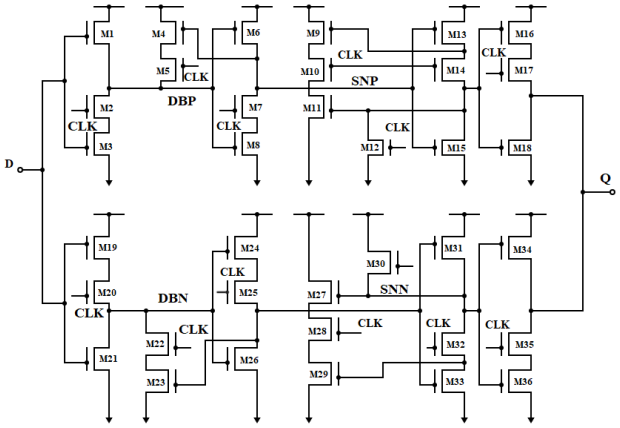

Figure 6. Schematic of the STCDET FF.

Dual-Edge Triggering by capturing data on both rising and falling edges of the clock, the flip-flop effectively doubles the data throughput without increasing the clock frequency. Complementary Paths top and bottom paths work in tandem to ensure that both Q and $\bar{Q}$ outputs are generated accurately and efficiently. Low-Power Design use of dynamic logic stages and careful transistor sizing helps minimize power consumption while maintaining high-speed operation.

The input-aware pre-charge technique improves energy efficiency by comparing the incoming data with the stored value before activating the pre-charge phase, avoiding unnecessary switching. This ensures correct flip-flop operation while reducing dynamic power. Further optimization is achieved by simplifying the transistor structure: PMOS transistors M11_1 and M11 are merged to deliver inverted data, but NMOS transistors M14 and M15 cannot be combined due to operational constraints. To maintain functionality, M15 is retained to prevent short-circuit current. Additionally, transistor M13 is removed as it is no longer needed its glitch-prevention role is rendered unnecessary by the low voltage at node N2, which eliminates the need for precharging, thus simplifying the design without compromising output accuracy.

STCDET flip-flops are less sensitive to clock skew since they capture data on both rising and falling clock edges, relaxing timing requirements and improving reliability. Their dual-edge operation also enhances noise immunity, reducing the risk of erroneous data capture compared to single-edge-triggered flip-flops. Additionally, the simplified timing behavior where one clock cycle handles two data transitions makes timing analysis more straightforward than in complex flip-flop designs, enabling easier integration and verification in digital systems[9].

4. Proposed TSPC Single Transistor Clocked Dual-Edge-Triggered Flip-Flop with Clock Gating and Power Gating

Figure 7 illustrates a dual-edge-triggered flip-flop (DFF) design that incorporates advanced power-saving techniques. The circuit is divided into two main sections: the Top Master-Slave Latch and the Bottom Master-Slave Latch, each responsible for capturing and storing data on opposite edges of the clock signal (CLK).

A. Operation of the Top FF in STC-DFF:

The Top Operation in the circuit diagram involves the Top Master Latch and the Top Slave Latch, which are part of a dual-edge-triggered flip-flop design. Here's a detailed breakdown:

The Top Master Latch is clocked using a Clocked PMOS (P2) and a Clocked NMOS (N2). These transistors are controlled by the CLK signal. when CLK is high, the Clocked PMOS (P2) turns off, and the Clocked NMOS (N2) turns on, allowing the input data (D) to be latched into the master latch. The data is stored in the cross-coupled inverters formed by transistors P1, N1, P14, and N7. This configuration ensures that the data is held stable until the next clock edge[10].

The output of the Top Master Latch is connected to the Midpoint (MID) node, which serves as the input to the Top Slave Latch. This node is crucial for transferring the latched data from the master to the slave during the appropriate clock phase. The Top Slave Latch is also a cross-coupled inverter structure formed by transistors P4, P8, N8, and N15. It is clocked using a Clocked PMOS (P15) and a Clocked NMOS (N15). When CLK transitions low, the Clocked PMOS (P15) turns on, and the Clocked NMOS (N15) turns off, allowing the data from the Midpoint (MID) to be transferred into the slave latch. The slave latch holds this data until the next clock cycle, ensuring that the output (Q or $\overline{Q}$) remains stable. The output of the Top Slave Latch is buffered through an inverter (formed by P6 and N6) to provide the final output ($\overline{Q}$). This inverter ensures that the output is driven with sufficient strength and maintains proper logic levels.

B. Operation of the Bottom FF in STC-DFF:

The Bottom Operation mirrors the top operation but is designed to handle the complementary data path. Here's how it works:

The Bottom Master Latch is clocked using a Clocked NMOS (N5) and a Clocked PMOS (P9). These transistors are controlled by the Clock signal. when CLK is low, the Clocked NMOS (N5) turns off, and the Clocked PMOS (P9) turns on, allowing the input data (D) to be latched into the master latch. The data is stored in the cross-coupled inverters formed by transistors P10, N10, P17, and N16. This configuration ensures that the data is held stable until the next clock edge.

The output of the Bottom Master Latch is connected to the Midpoint (MID_n') node, which serves as the input to the Bottom Slave Latch. This node is crucial for transferring the latched data from the master to the slave during the appropriate clock phase. The Bottom Slave Latch is also a cross-coupled inverter structure formed by transistors P11, P12, N12, and N18. It is clocked using a Clocked PMOS (P17) and a Clocked NMOS (N17). When CLK transitions high, the Clocked PMOS (P17) turns on, and the Clocked NMOS (N17) turns off, allowing the data from the Midpoint (MID_n') to be transferred into the slave latch. The slave latch holds this data until the next clock cycle, ensuring that the output (Q) remains stable. the output of the Bottom Slave Latch is directly connected to the final output (Q). This ensures that the output reflects the correct state based on the input data and the clock signal[11].

Dual-Edge-Triggering enables a synchronous circuit to respond to both transitions of the clock waveform. By designing storage elements such as flip-flops or latches to activate on either edge, the system can process data twice per clock cycle. This is achieved through techniques like edge multiplexing, where two separate latch paths are controlled

by delayed or inverted clock signals, ensuring correct timing and data integrity. The result is enhanced performance with minimal increase in power or complexity, making it a valuable strategy in modern digital design. Complementary Path The top and bottom paths work in tandem to ensure that both Q and $\bar{Q}$ outputs are generated accurately and efficiently.

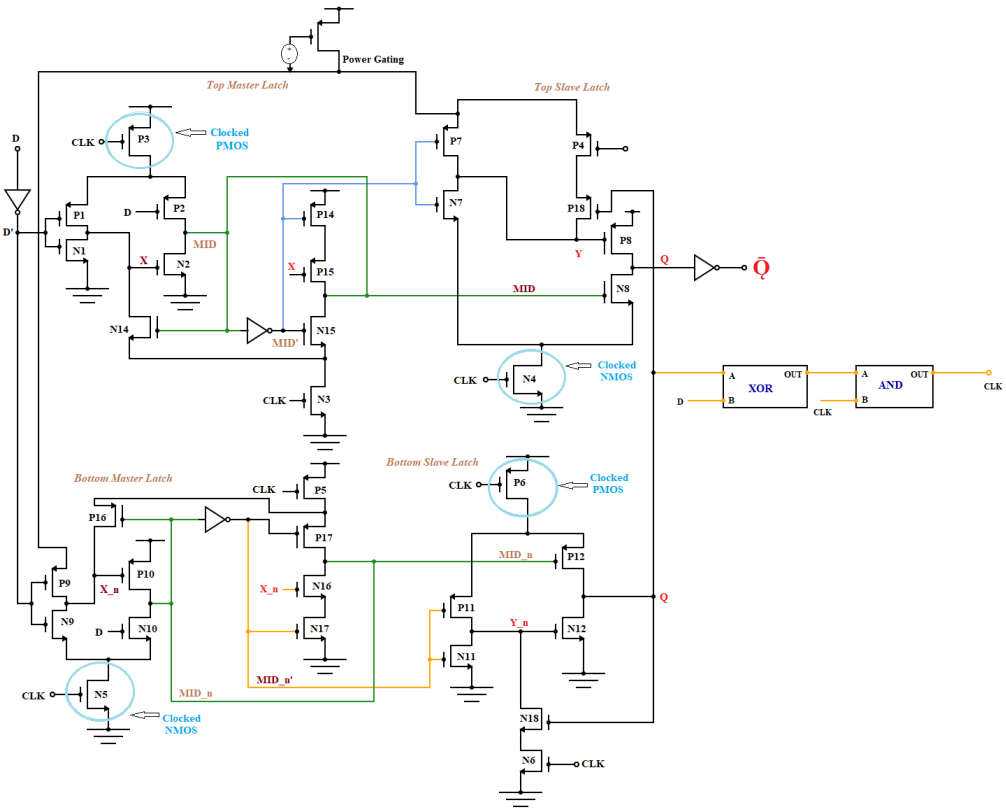

Figure 7. Proposed TSPC single transistor clocked Dual-Edge Triggered Flip-Flop with Clock Gating and Power Gating.

5. Schematic Diagram and Results

A static contention-free single-phase-clocked flip-flop in 45 nm for low-power applications using dual-edge-triggered flip-flop is a sequential logic circuit that captures the input data (D) on both the rising (positive) and falling (negative) edges of the clock signal. Unlike conventional flip-flops that respond to only one edge (typically the rising edge), this design effectively doubles the data throughput without increasing the clock frequency [12].

The schematic for the TSPC flip-flop with clock gating involves applying a signal A to both the gate of the PMOS transistor and the source of the NMOS transistor (**Figure 8**). For the PMOS, the gate signal is complemented (denoted as A'), and when multiplied with the source signal A, the drain terminal output evaluates to 0 due to the Boolean law A.A' = 0. Similarly, for the NMOS, the gate signal A is multiplied with the source signal B, resulting in an output at the drain terminal of A.B. Since the drain terminals of both the PMOS and NMOS are connected together, their combined output simplifies to 0 + A.B = A.B, effectively implementing an AND gate operation. This configuration ensures that the logic function is correctly realized while maintaining the desired circuit behavior.

A similar operational principle applies from the AND gate to the XOR gate. From the schematic, here 2 PMOS and 1 NMOS is utilized to satisfy the logical operation of XOR. The drain of terminal of NMOS would results in 0 as the product of gate NMOS's source terminal is B, and its terminal is GND [Logic 0]. For the first PMOS drain would result in A'B whereas the other PMOS drain terminal would results in AB'. As all the drain terminals are connected together the aggregate value of these drain terminal is considered as output of XOR gate which results in 0+A'B+AB'. This satisfies our XOR logical operation.

In the modified TSPC design with Auto Gated Clock

Gating, an XOR and AND gate combination forms the clock gating module, producing a conditioned clock signal (CK) (**Figure 9**). This signal depends on the main clock (CLK), data input (D), and previous output, allowing clock pulses to be disabled when no data change occurs. By using CK to drive the slave latches instead of the raw clock, switching activity is reduced, cutting dynamic power consumption while maintaining correct circuit operation [13].

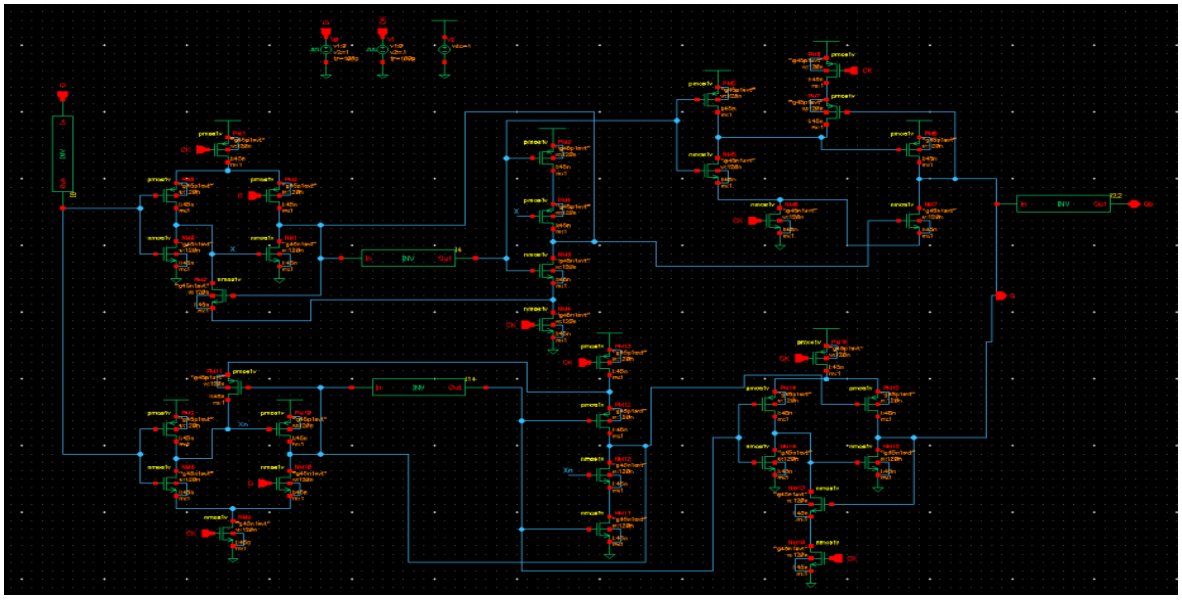

Figure 8. Schematic of proposed TSPC Flipflop.

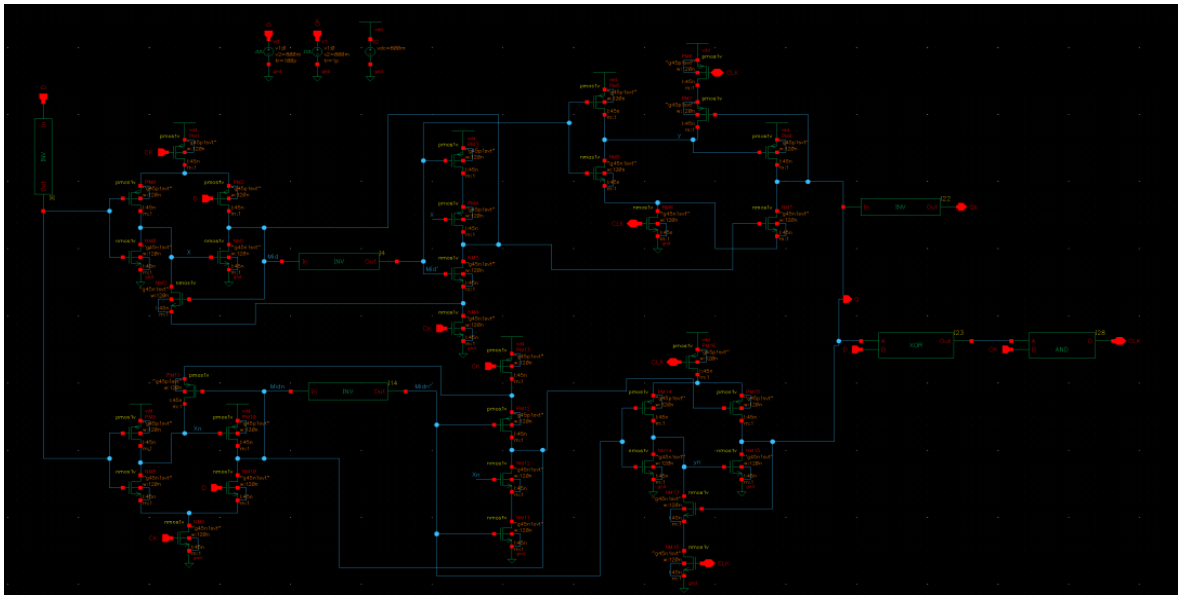

Figure 9. Modified schematic of TSPC with clock gating.

To reduce power consumption, the circuit operates in active or sleep mode based on the output of the XOR and AND gates, which detect when data transitions occur. Unlike the conventional design that remains always active, the proposed flip-flop enables clock gating only when a data change is needed, minimizing unnecessary switching. Additionally, power gating is employed by inserting a switch (such as a PMOS transistor) between the power supply and the circuit block (**Figure 10**). This switch, controlled by a power management unit, disconnects the supply during idle periods, significantly reducing leakage and dynamic power without affecting functional integrity [14].

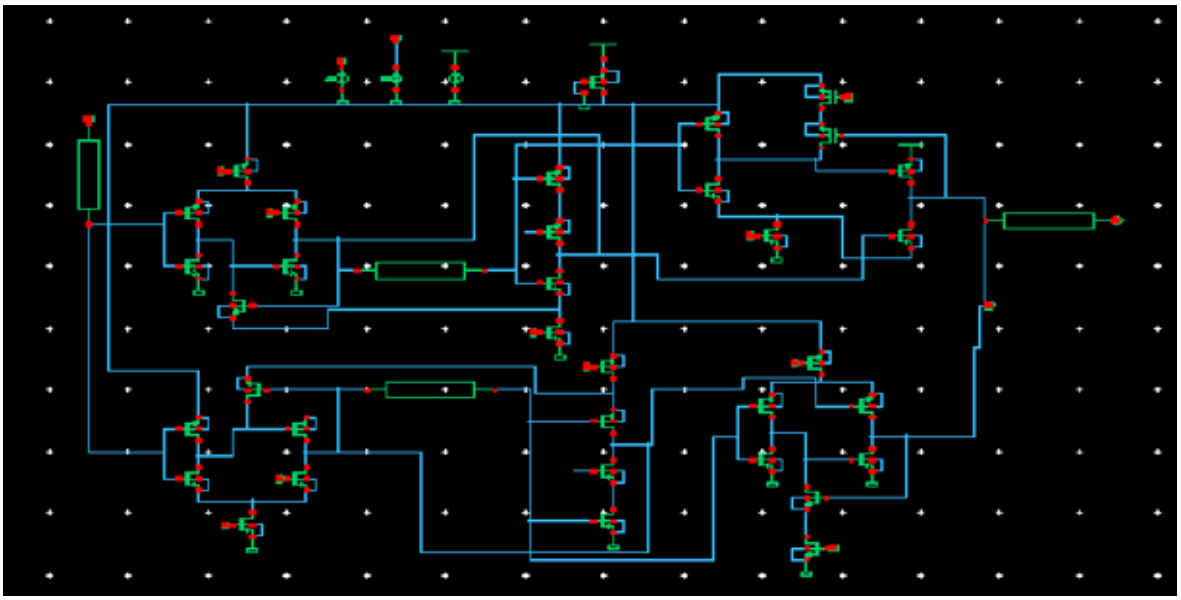

Figure 10. Modified schematic of TSPC with power gating.

The power gating technique illustrated in the diagram involves adding a PMOS transistor as a switch between the VDD supply and the circuit. Unlike the previous design where VDD was directly connected, this approach controls power delivery by turning the PMOS transistor on only when the circuit is active. When the circuit is idle, the transistor cuts off the power supply, significantly reducing leakage and dynamic power consumption. Although only one additional transistor is introduced, it greatly enhances power efficiency without significantly impacting the overall design complexity. This makes power gating a highly effective method for optimizing power usage in low-power integrated circuit designs.

The waveform in the proposed diagram (**Figure 11**) illustrates the operation of a dual-edge triggered circuit. In this configuration, the output responds to both the rising and falling edges of the input signal. Whenever the input transitions to a high state, the output also goes high, and when the input goes low, the output follows accordingly. This behavior occurs regardless of whether the clock pulse is rising or falling, enabling the circuit to capture input changes on both edges of the clock cycle, thereby increasing its responsiveness and data throughput.

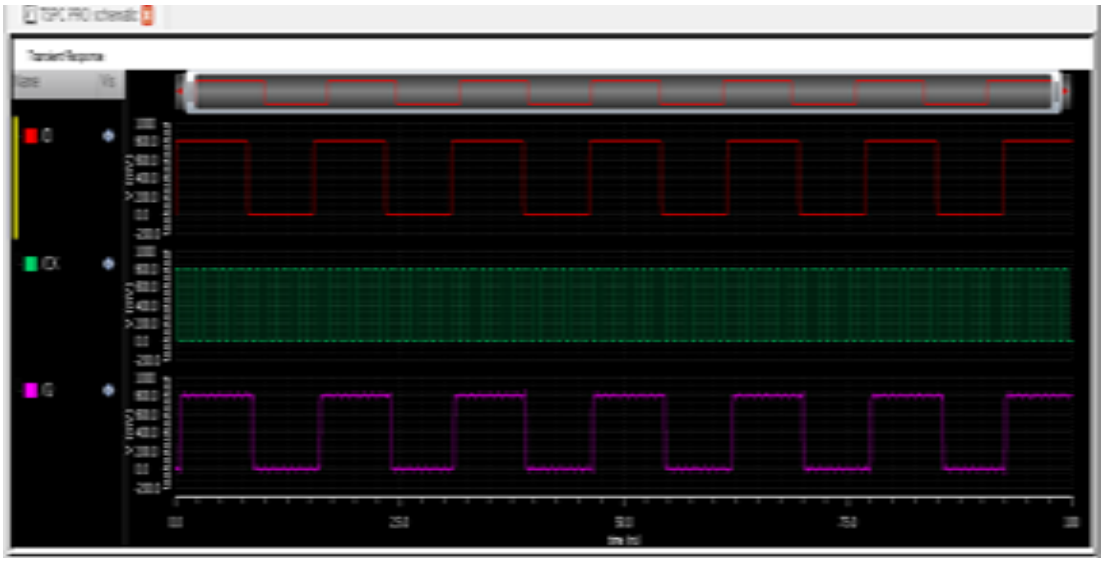

Figure 11. Result of waveform for proposed STCDET.

In this design, clock gating is implemented to optimize power consumption without altering the functionality of the output. The output waveform continues to follow the input clock pulses responding to both high and low transitions just as it did without clock gating (**Figure 12**). The primary changes introduced by clock gating are reduced power consumption and a slight impact on signal delay, while the logical behavior and output timing remain unchanged. This makes clock gating an effective technique for minimizing dynamic power without affecting circuit performance.

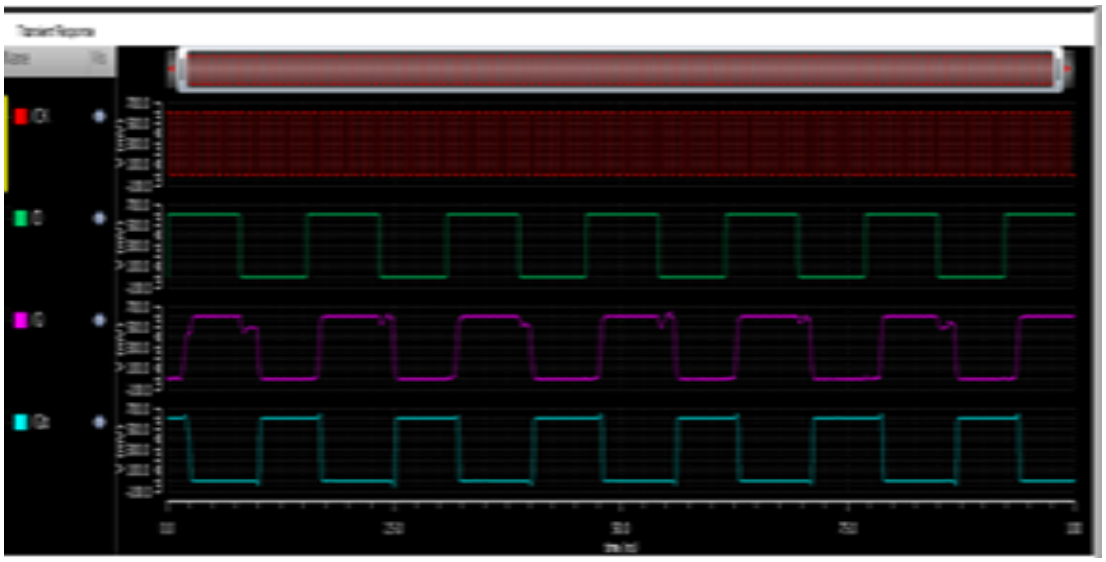

Figure 12. Result of waveform for modified TSPC with clock gating.

As shown in the **Figure 13**, the output waveform of the flip-flop remains unchanged after applying power gating. The signal behavior closely matches the previous case, maintaining the same logic transitions and timing. The only differences are observed in power consumption and propagation delay, where power is significantly reduced during inactive modes due to the isolation of the power supply. Thus, power gating improves energy efficiency without altering the functional output of the flip-flop.

The comparison of power consumption graph is shown in the figure the power of proposed diagram is more 345.2 Nanowatts (nW), so coming to next clock gating power is going to reduce to 273.4 Nanowatts (nW), so finally after applying power gating the huge difference in power consumption as you can observe on the graph it is 83.14 Nanowatts (nW) it is fully decreased[15].

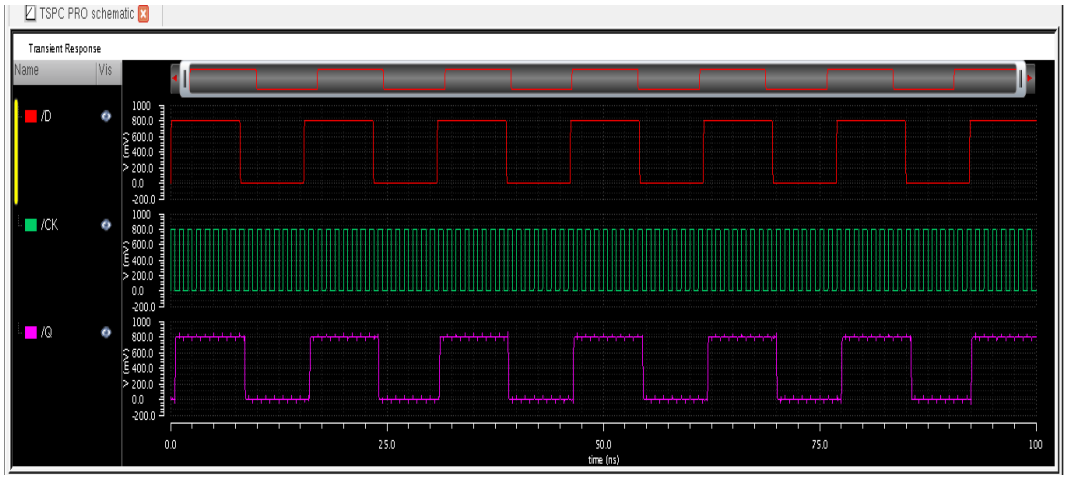

Figure 13. Result of waveform for modified TSPC with power gating.

6. Comparison & Analysis

The comparison of area all the three methods proposed area is 42 after applying the clock gating its 49 & in power gating its 43 and the comparison of delay shown in graph the delay of proposed is 0.498 nanosecond (ns), coming to next clock gating it is small change in that 0.025 nanosecond (ns) after the power gating its 0.553 nanosecond (ns) as shown in **Figures 14** and **15**[16].

Table 2 presents a comparative analysis of the proposed design with two established techniques clock gating and power gating in terms of key performance metrics. The proposed approach consumes 345.2 nanowatts (nW), occupies an area of 42 units, has a delay of 0.498 nanoseconds (ns), and achieves a power-delay product (PDP) of 171.90 femtojoules (fJ). In contrast, clock gating demonstrates lower power usage at 273.4 Nanowatts (nW) and significantly reduced delay at 0.025 ns, though it results in a much higher PDP of 6.835 femtojoules (fJ). Power gating offers the lowest power consumption at 83.14 Nanowatts (nW) but suffers from a longer delay of 0.345 ns and a PDP of 45.976 femtojoules (fJ), indicating a trade-off between power efficiency and speed.

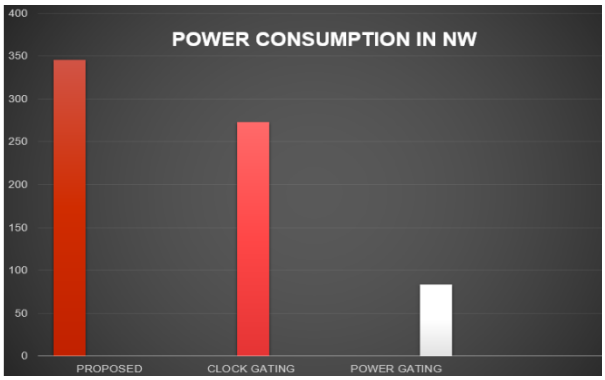

Figure 14. Comparison of power consumption.

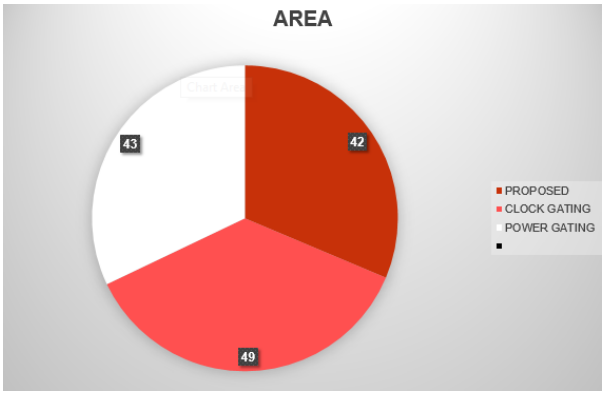

Figure 15. Comparison of area.

Table 2. Performance comparisons.

Design	Power Consumption	Area	Delay	PDP
Proposed	345.2 Nanowatts (nW)	42	0.498 nanosecond (ns)	171.90 femtojoules (fJ)
Clock gating	273.4 Nanowatts (nW)	49	0.025 nanosecond (ns)	6.835 femtojoules (fJ)
Power gating	83.14 Nanowatts (nw)	43	0.345 nanosecond (ns)	45.976 femtojoules (fJ)

The delay performance of various power management techniques is shown in **Figure 16**. The proposed method[1] exhibits the highest delay due to additional circuitry introduced for power optimization. In contrast, clock gating[2] achieves minimal delay by selectively disabling clock signals to idle components. Power gating[3], while effective in reducing leakage power, introduces moderate delay due to sleep transistor switching overhead.

The power delay product (PDP), a key metric for evaluating energy efficiency in digital circuits, is compared across three techniques in **Figure 17**. The proposed method[1] exhibits the highest PDP due to increased dynamic power consumption from additional control logic and switching activity. In contrast, clock gating[2] achieves the lowest PDP by reducing dynamic power through clock signal disabling during idle periods. Power gating[3] offers a moderate PDP, balancing leakage reduction with the overhead of sleep transistor activation.

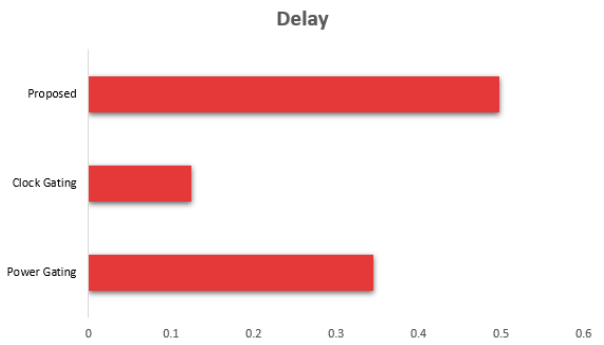

Figure 16. Comparison of delay.

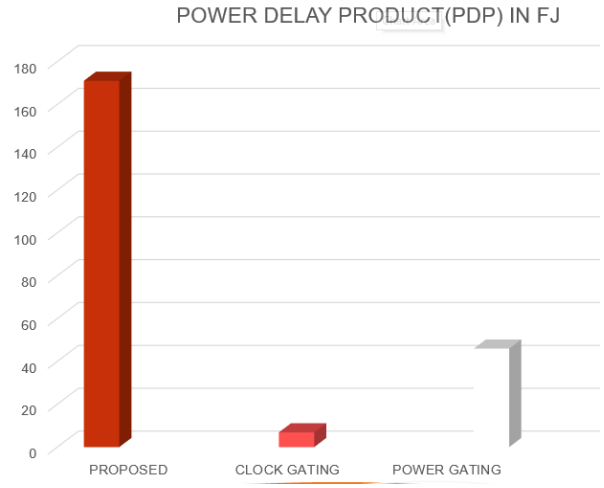

Figure 17. Comparison of power delay product.

In the comparison of proposed is huge number 171.90 j comparing to our clock gating it is reduced to 6.835 j & after applying the power gating its increased to 45.97j but compare to proposed its less only.

7. Conclusions

In conclusion, the proposed low-power TSPC flip-flop integrates three key energy-saving techniques auto-gated clock gating, power gating and redundant-transition suppression to significantly reduce both dynamic and leakage power consumption. By intelligently disabling the clock signal when not needed, cutting off power to idle circuit blocks, and eliminating unnecessary internal switching activities, the design achieves substantial power savings without compromising performance or reliability. This makes it particularly suitable for energy-constrained applications such as portable and IoT devices, where minimizing power usage is critical. The synergistic combination of these techniques demonstrates a promising approach for developing high-efficiency sequential circuits in modern low-power VLSI systems.

Author Contributions

Conceptualization, B.R.K.; methodology, B.R.K.; software, B.R.K.; validation, B.R.K., P.K. and E.J.A.; formal analysis, B.R.K.; investigation, P.K.; resources, P.K.; data curation, P.K.; writing—original draft preparation, B.R.K. and P.K.; writing—review and editing, B.R.K., P.K., E.J.A. and K.N.R.; Visualization, K.N.R.; project supervision, K.N.R.; project administration K.N.R.; All authors have read and approved the final published version of the manuscript.

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Data Availability Statement

The data supporting the findings of this study are available from the corresponding author upon reasonable request. All simulation results, design schematics, and performance metrics reported in this paper were generated using standard Cadence Virtuoso and it can be reproduced based on the methodology and parameters described in the article. Due to the constraints of intellectual property and the proprietary nature of certain design configurations, the raw simulation datasets have not been deposited in a public repository. However, anonymized and non-proprietary summary data, along with supporting figures and tables, are included in the manuscript and supplementary materials. No new experimental data were generated involving human subjects or sensitive information.

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Conflicts of Interest

The authors declare no conflict of interest. The research presented in this paper was conducted independently, and there are no financial, personal or professional relationships that could be perceived as influencing the results or conclusions reported. The funders had no role in the design of the study in the collection, analyses or interpretation of data in the writing of the manuscript or in the decision to publish the results.

References

[1] Moreau, L., Dekimpe, R., Bol, D., 2019. A 0.4V 0.5fJ/cycle TSPC Flip-Flop in 65nm LP CMOS with Retention Mode Controlled by Clock-Gating Cells. Proceedings of the 2019 IEEE International Symposium on Circuits and Systems (ISCAS); Sapporo, Japan; 26–29 May 2019.

[2] Atzori, L., Iera, A., Morabito, G., 2010. The Internet of Things: A Survey. Computer Networks. 54(15), 2787–2805.

[3] Kumar, S., 2019. Design and Analysis of SEU Hardened Latch for Low Power and High-Speed Applications. Journal of Low Power Electronics and Applications. 9(3), 21.

[4] Tekeste, T., Saleh, H., Mohammad, B., et al., 2018. A Nano-Watt ECG Feature Extraction Engine in 65-nm Technology. IEEE Transactions on Circuits and Systems II: Express Briefs. 65(8), 1099–1103.

[5] Pullini, A., Rossi, D., Loi, I., et al., 2019. Mr. Wolf: An Energy-Precision Scalable Parallel Ultra-Low Power SoC for IoT Edge Processing. IEEE Journal of Solid-State Circuits. 54(7), 1970–1981.

[6] Vo, M.-H., Dao, A.-Q., 2015. Dual-Switch Power Gating Technique with Small Energy Loss, Short Crossover Time, and Fast Wake-Up Time for Fine-Grain Leakage Controlled VLSIs. Proceedings of the 2015 International Conference on Advanced Technologies for Communications; Ho Chi Minh City, Vietnam; 14–16 October 2015. pp. 264–269.

[7] Kawai, N., Takayama, S., Masumi, J., et al., 2014. A Fully Static Topologically-Compressed 21-Transistor Flip-Flop with 75% Power Saving. IEEE Journal of Solid-State Circuits. 49(11), 2526–2533.

[8] Ding, Li., Mazumder, P., Srinivas, N., 2001. A Dual-Rail Static Edge-Triggered Latch. ISCAS 2001. Proceedings of the ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196); Sydney, NSW, Australia; 6–9 May 2001.

[9] Hirata, A., Nakanishi, K., Nozoe, M., et al., 2005. The Cross Charge Control Flip-Flop: A Low-Power and High-Speed Flip-Flop Suitable for Mobile Application SoCs. Proceedings of the Digest of Technical Papers Symposium on VLSI Circuits; Kyoto, Japan; 16–18 June 2005. pp. 306–307.

[10] Shandilya, R., Sharma, R.K., 2017. High Speed Low Power Dual-Edge Triggered D Flip-Flop. Proceedings of the 2017 International Conference on Intelligent Computing and Control (I2C2); Coimbatore, India; 23–24 June 2017.

[11] Shin, J.L., et al., 2013. The Next Generation 64b SPARC Core in a T4 SoC Processor. IEEE Journal of Solid-State Circuits. 48(1), 82–90.

[12] Teh, C.K., Fujita, T., Hara, H., et al., 2011. A 77% Energy-Saving 22-Transistor Single-Phase-Clocking D-Flip-Flop with Adaptive-Coupling Configuration in 40 nm CMOS. Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers; San Francisco, CA, USA; 20–24 February 2011. pp. 338–339.

[13] Cai, Y., Savanth, A., Prabhat, P., et al., 2019. Ultra-Low Power 18-Transistor Fully Static Contention Free Single-Phase Clocked Flip-Flop in 65-nm CMOS. IEEE Journal of Solid-State Circuits. 54(2), 550–559.

[14] Kim, Y., Jung, W., Lee, I., et al., 2014. A Static Contention-Free Single-Phase-Clocked 24T Flip Flop in 45 nm for Low-Power Applications. Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 9–13 February 2014; pp. 466–467.

[15] Cerqueira, J.P., Repetti, T.J., Pu, Y., et al., 2020. Catena: A Near-Threshold, Sub-0.4-mW, 16-Core Programmable Spatial Array Accelerator for the Ultralow-Power Mobile and Embedded Internet of Things. IEEE Journal of Solid-State Circuits. 55(8), 2270–2284.

[16] Saha, S., Kumar, U.S., Baghini, M.S., et al., 2017. A Nano-Electro-Mechanical Switch Based Power Gating for Effective Stand-by Power Reduction in FinFET Technologies. IEEE Electron Device Letters. 38(5), 681–684.