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An Improved Power Efficient Clock Pulsed D Flip-flop Using Transmission Gate

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ABSTRACT

Recent digital applications will require highly efficient and high-speed gadgets and it is related to the minimum delay and power consumption. The proposed work deals with a low-power clock pulsed data flip-flop (D flip-flop) using a transmission gate. To accomplish a power-efficient pulsed D flip-flop, clock gating is proposed. The gated clock reduces the unnecessary switching of the transistors in the circuit and thus reduces the dynamic power consumption. The clock gating approach is employed by using an AND gate to disrupt the clock input to the circuit as per the control signal called Enable. Due to this process, the clock gets turned off to reduce power consumption when there is no change in the output. The proposed transmission gate-based pulsed D flip-flop's performance with clock gating and without clock gating circuit is analyzed. The proposed pulsed D flip-flop power consumption is 1.586 μw less than the without clock gated flip-flop. Also, the authors have designed a 3-bit serial-in and parallel-out shift register using the proposed D flip-flop and analyzed the performance. Tanner Electronic Design Automation tool is used to simulate all the circuits with 45 nm technology.

Keywords: Pulsed D flip-flop; Clock gating; Low power; Shift register; Transmission gate

1. Introduction

The main concern with VLSI circuits is achieving low power and compact battery size with a long life. Area, power, speed, and performance are all critical parameters for VLSI designers to con-

sider while optimizing their designs^[1-4]. Flip flops are the major building blocks of digital circuits and also consume around 80% of the total power consumption in the circuits. Therefore, reducing the power consumption of flip-flops can signifi-

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cantly reduce the power consumption of digital systems [5]. Any circuit's overall power consumption will include both static and dynamic power. In VLSI circuits, power gating, clock gating, adiabatic method, and other approaches are utilized to reduce static and dynamic power consumption. One of the most common strategies for power optimization in CMOS devices is clock gating [1]. Almost 50% of the dynamic power is consumed by the clock distribution network in processors and clock gating can be used at several levels of the hierarchy in VLSI design and almost 50% of the dynamic power is consumed by the clock distribution network in integrated circuits. It is feasible to turn off the clock signal that drives a large functional unit, lowering power consumption on both its internal nodes and the clock line.

Pulsed Flip-Flops (P-FF): Pulsed flip-flops are used in high speed circuits and take an important role in power reduction. Short duration pulses are generated and used to trigger the flip-flops instead of level or edge triggering. P-FFs consist of a single latch structure and a clock pulse generator (PG). If the width of the clock pulse is sufficiently narrow, the P-FF acts like a Master-Slave Flip-Flops (MS-FF) with less timing overhead. Jhon K et al. showed that several pulse triggered flip-flop architecture for high speed allocations [5]. PF-FFs can be classified as implicit and explicit type based on the way of pulse generation. In implicit style, the pulse generation part is inbuilt into the latch structure and in explicit it is external to the latch structure. In explicit pulsed flip-flops, the pulse generation structure can be common among neighboring flip-flops and saves chip area.

Transmission Gate: The parallel connection of nmos and pmos forms the Transmission Gate (TG). The transmission gate's on or off condition is controlled by the nmos and pmos gate inputs. The gate is in on condition when nmos transistor gate gets Clk input and pmos transistor gate gets Clkb input and TG the circuit is shown in **Figure 1**.

TGs are bilateral switches since the input and output are interchangeable. TGs are used to form D latch and

D flip-flops in logic circuits. The positive D latch using the transmission gate is shown in **Figure 2**.

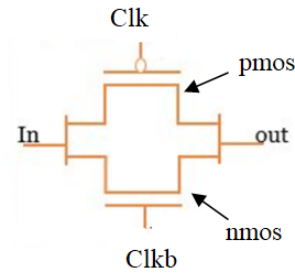


Figure 1. Transmission gate.

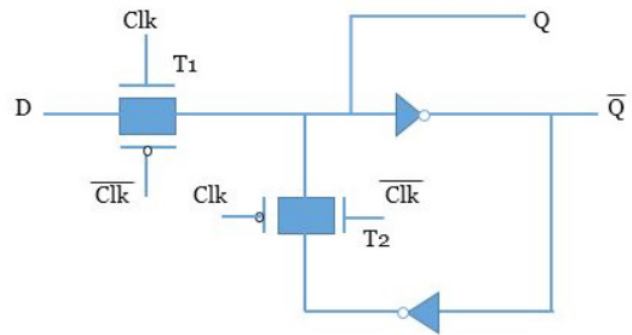


Figure 2. Transmission gate based D latch.

It consists of two TGs and two inverters. When Clk = high, T1 is ON and T2 is OFF, so output (Q) directly follows the input (D). Otherwise, the output is the stored values in the latch.

The proposed work deals with transmission gate based pulsed D flip-flop design with clock gating for power reduction. The paper is organized as follows. Section 2 describes the related work and Section 3 describes the proposed clock gated transmission gate based D flip-flop and Section 4 describes the implementation of a shift register using the proposed D flip-flop. Section 5 discusses the results and Section 6 gives the conclusions.

2. Related work

Ultra-low power pulse-triggered carbon nanotube field-effect transistor (CNTFET) based flip-flop is proposed by Karim et al. [6] for low power applications. The author used signal feed through technique and also optimized the discharging path to reduce the delay time for the '1' to '0' transition. The proposed

design is also area efficient, since the number of transistors used is less when compared to the other pulse triggered flip-flop schemes. An explicit type double edge pulse-triggered flip-flop is designed by Singh et al. [7]. The author used Exor gate based pulse generator to obtain a short pulse at the rising edge and falling edge of the clock signal. The designed flip-flop has less power delay product and is more suitable for high speed applications. Phyu et al. designed the pulse triggered flip-flop using static latch and dynamic pulse generator [8]. The author used explicit type double edge triggering approach. Ameen et al. proposed another explicit type pulse triggered flip-flop based on data feed through scheme [9]. The proposed data feed through scheme reduces the long discharge path in conventional explicit pulse triggered flip-flops and is also suitable for high speed applications. John K. [10] proposed an implicit type pulse triggered flip-flop by making conditional enhancement in width and height of the triggering pulses by using an additional pmos transistor in the structure for high speed applications. J.F.Lin et al. [11] proposed an explicit type pulsed flip-flop by using True single-phase clock latch based on a signal feed-through scheme.

Karimni [12] proposed an ultra low pulse triggered flip-flop with optimized leakage power. The author used transmission gate to control the input data and the leakage power. Also, the Pulse Generator (PG) is modified to reduce the number of required transistors and the clock pulse delay. Panahifar, E. & Hassanzadeh designed a signal feed-through flip-flop that uses a pass transistor to feed input data directly to the output and minimizes the dynamic power [13]. Another efficient high speed conditional feed through pulsed flip-flop was proposed by Pan.D et al. [14]. Pulsed flip-flop using a transmission gate is proposed by Prakalya et al. [15]. They used current mode distribution of clock pulses than the conventional voltage mode operation. Consoli, E. et al. designed a modified transmission gate based Master Slave Flip-Flop (MS F/F) to minimize the delay in the classical transmission gate based approach [16]. Islam R. et al. [17] proposed a current mode pulsed flip-flop combined

with a current mode signaling transmitter, which reduces the power consumption of clock distribution networks more than the voltage mode distribution of clock signal.

Clock gating is one of the efficient methods in clock power reduction while the input signal switching activity is low [18,19]. John K et al. discussed the effect of clock gating on conditional pulsed flip-flops and analyzed in their work [20]. Sharma, D. K designed and analyzed different clock gating circuits such as latch based, flip-flop based and gate based [21]. The author analyzed the circuits in terms of delay, power and area and proved that gate based clock gating circuits are more power efficient [21]. A latch-based clock gating technique is used in the design of SRAM and sequential counter and verified the power reduction in the work [22].

3. Proposed work

3.1 Clock gating

The static (leakage) power grows dramatically with each generation of technology, dynamic power still dominates the total power dissipation of general-purpose microprocessors [2]. The reduction in transistor size, interconnect optimization, applying gated clock, applying variable threshold voltages, and the management of dynamic supply voltage are all effective circuit strategies for reducing dynamic power usage. Clock gating is one of the efficient methods in clock power reduction when the input signal switching activity is low.

The clock gating approach needs an additional logic circuit to generate a clock enabling signal [19,21,23]. The logic circuit compares the input and output of the latch and if there is any change in the output, which will be enabled only when the need for output changes to logic 0 or 1 value according to the circuit design. The clock gating approach is used to prevent unnecessary clock pulses from being sent to the circuit when there is no need for output change. For example, already flip-flop has output 1, if the next input bit is 1 then no need to apply the clock pulse to the flip-flop. This will reduce the unnecessary

switching of the circuit capacitance and thus reduces the dynamic power consumption. Moreover, the toggling nature of the clock consumes more power in registers.

In flip-flops, the switching activity is increased due to the transition from 0 to 1 and 1 to 0, and they require more power. The first step in implementing clock gating is to identify the location (module) which consumes large power. The next step is to study the switching activity of the module and based on that designing of a control logic circuit that produces the enable signal. The enable signal is used to turn off and on the clock signal which is going to be applied at that location. When there is no change in the output of a particular register or flip-flop, then that unit does not require a clock pulse, since the unit is going to maintain the same output. The clock gating approach cuts the clock pulse to that particular register or flip-flop and thus in turn saves the dynamic power dissipation. In a sequential circuit, the simple solution is to cut the clock pulses which are not going to change the output state of the circuit. This reduces power consumption. The clock gating to the flip-flop block diagram is shown in **Figure 3**.

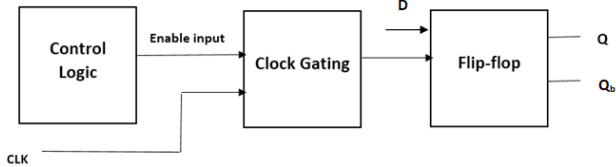


Figure 3. Clock gating technique to the flip-flop.

3.2 Flow chart for clock gating

The flowchart shown in **Figure 4** shows the simple clock gating method. The clock pulses are applied to the circuit whenever the clock and enable input both are in logic '1' condition. If the enable signal is logic '0' then the clock pulse is blocked to the circuit. Clock gating is a simple structure and easy to implement. Any of the following gates can be utilized in a gated clock gating approach. AND, OR, and NOR gates are the three gates that are used in clock gating. Only when both inputs reach a high value does the AND gate on. Because of the short

transition period from high to low, when enabling pin = 1, the counter in negative edge triggering type increments by one count. When the enable pin = 1 during the positive edge of the clock, there is a long fall time, which results tiny glitches (short duration clock pulses) and the circuit produces output with an error. The AND gate is mostly used for activating negative edge triggering circuits.

There are two inputs, Enable and Clock are given to the AND gate. The circuit operation is as follows. When the Enable is low and the Clock is low then the transistor T1, T4, and T6 are in ON condition and the T2, T3, T5 are in OFF, so the output is low. When the Enable is low and the Clock is high the transistors T1, T3, and T6 are in ON condition the transistor T2, T4, and T5 are in OFF condition, so the output is low. Similarly, when the Enable is high and the Clock is low, the transistors T2, T4, and T6 are in ON condition and the transistor T1, T3, and T5 are in OFF condition and the output is low. When the Enable is high and the Clock is high the transistor T2, T3, and T5 are in ON condition and the transistors T1, T4, and T6 are in OFF condition and the output is high. The clock gating circuit output is shown in **Figure 6**. Whenever the Enable and the Clock both are set to HIGH then the output is HIGH and the gated clock is given to the proposed D flip-flop.

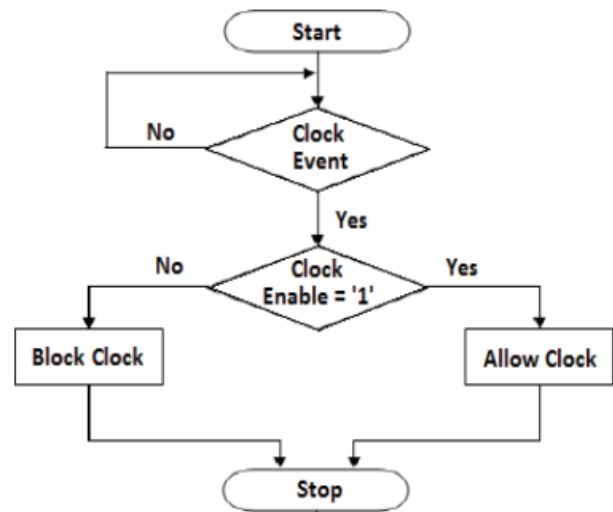


Figure 4. Flowchart of clock gating.

The proposed clock gating circuit is shown in **Figure 5**.

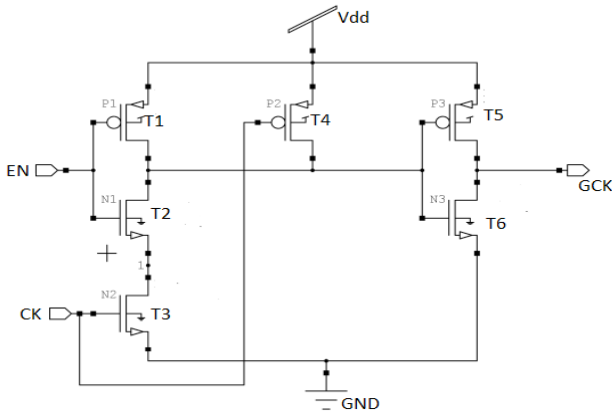


Figure 5. Schematic of AND clock gating.

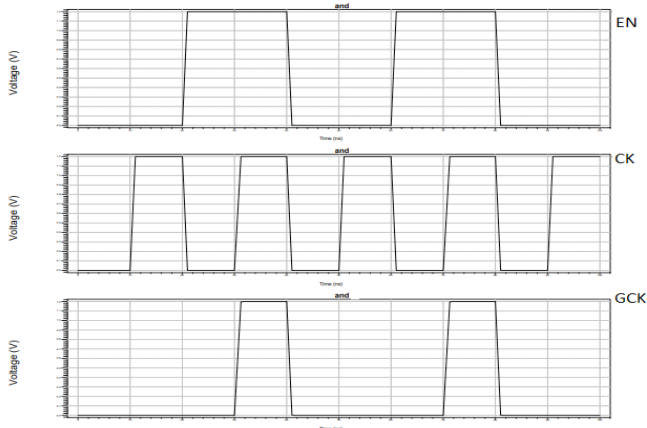


Figure 6. Waveforms of AND Clock gating.

3.3 Transmission gate based D flip-flop

Transmission gate logic is one of the additional ways to reduce power consumption by using more power-efficient circuitry to implement the D flip-flop [8,24]. The transmission gate logic is used to construct a flip-flop register stage and is also used at the input stage in memristors [25]. The Figure 7 shows a leading-edge triggered D flip-flop without Set, Reset, or Clear signals with the clock signal. D is the input signal and Clk and Clkb denote clock and inverted clock signals respectively.

The D pin is used to provide input in a flip-flop. Transmission gates are equipped with clock pulses that make the transmission gates on and off. When the Clk = 1 and Clkb = 0, then the conditions of TGs are as follows. TG1 = Off, TG2 = On, TG3 = On and TG4 = Off and the data stored in the latch (N1) will be trans-

ferred to the output. When Clk = 1 and Clkb = 0, then TG1 = On, TG2 = Off, TG3 = Off and TG4 = On and the data at D will be transferred to the first latch (node N1). The circuit acts as a master-slave flip-flop. The modified flip-flop circuit using an efficient clock distribution network is shown in Figure 8 [15].

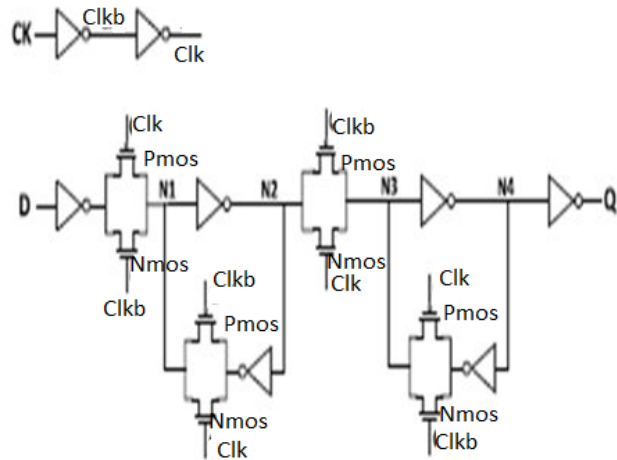


Figure 7. Schematic of transmission gate-based D flip-flop.

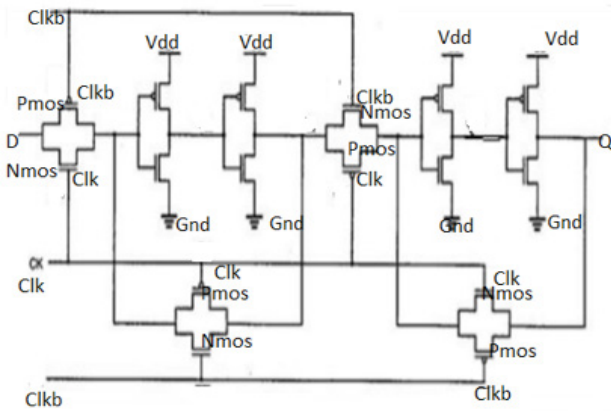


Figure 8. Schematic of TG-based D flip-flop with the clock distribution network.

The proposed flip-flop with the gated clock is shown in Figure 9. Whenever the enable and the clock are set to HIGH then only the output is HIGH. The gated clock is given to the proposed D flip-flop. As in Figure 9, the gated Clk is applied to the inverter to obtain the Clk and Clkb signals.

In the proposed circuit D flip-flop is implemented using 24 transistors. The clock gating logic is added to the D flip-flop, which increases the complexity of the circuit, but the power consumption is reduced be-

cause of the AND clock gating logic. The transistors T1 and T2 combined to form a transmission gate i.e., TG1. The transistors T5 and T6 combined to form a transmission gate i.e., TG2 and the transistors T9 and T10 combined to form a transmission gate named TG3. The transistors T13 and T14 form transmission gate, named TG4. If D input is High and the clock is High, then the gated clock output will be one. That is $Clk = 1$ and $Clkb = 0$. Now, the TG1 and TG4 will be in on condition and TG2 and TG3 will be in off condition. The input D is transmitted to the first latch and the output is the data stored in the second latch. When the gated clock is zero, that is $Clk = 0$ and $Clkb = 1$, then the TG1 and TG4 will be in off condition and TG2 and TG3 will be in on condition and the data in the first latch is moved to the second latch, and whenever clock one, the data will be made available at the output.

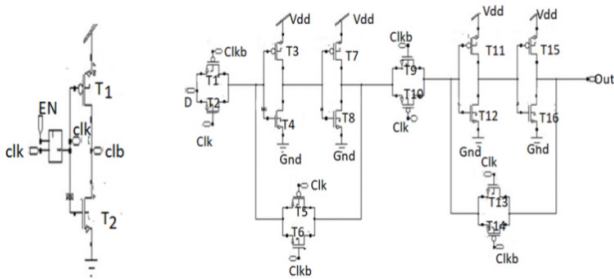


Figure 9. Schematic of proposed transmission gate based D flip-flop with clock gating.

Figure 10 shows the proposed D flip-flop output waveforms with clock gating.

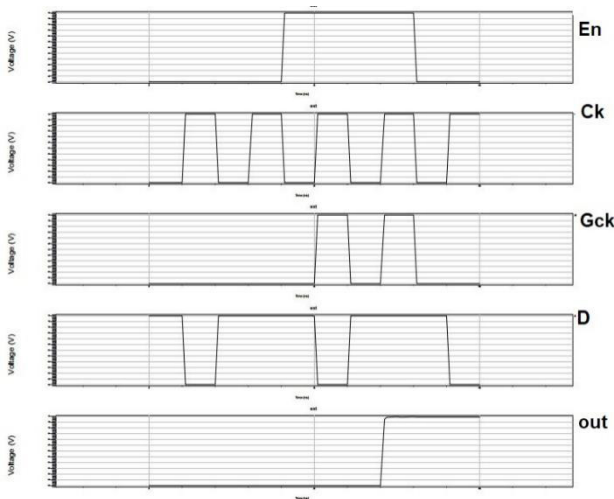


Figure 10. Waveforms of TG-based D flip-flop with AND clock gating.

4. Serial in parallel out shift register using proposed D flip-flop

A 3-bit serial-in and parallel-out shift register is designed using the proposed pulsed transmission gate based D flip-flop with clock gating. Shift registers consist of three proposed D flip-flops. Each flip-flop module is with clock gating circuit. Clock pulses and enable signal are applied to all the flip-flops and the data stored in the flip-flops are moved based on the gated clock output. The gated clock becomes high (logic '1'), when both the Clk and enable input are high. The shift register circuit is shown in Figure 11. The inputs D and EN (Enable) and CK (Clk) are given as follows.

input D: 1 1 1 0 1 1 1 0 1 1
 input EN: 1 1 0 0 1 1 0 0 1 1.
 Clock: 0 1 0 1 0 1 0 1 0 1
 Gated clock output: 0 1 0 0 0 1 0 0 0 1

The data shifting with the gated clock condition ($En=1$ & $Clk=1$) is shown in Figure 12.

As shown Figure 12, V(3) becomes '1' during the first gated clock pulse and V(2), V(1) becomes '1' during the second and third gated clock pulses.

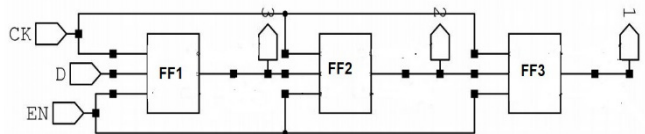


Figure 11. Schematic of three bit shift register with clock gating.



Figure 12. Waveforms of three-bit shift register.

5. Implementation results in tanner tool

The proposed transmission gate based D flip-flop with clock gating circuit and shift register circuits discussed in Sections 3 and 4 are simulated and their performance is measured using tanner tool with 45 nm technology.

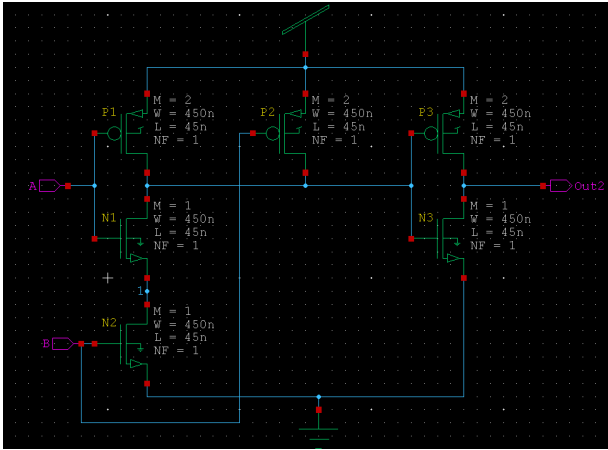


Figure 13. Schematic of AND clock gating in tool.

Figure 13 shows the AND gate clock gating circuit implementation of the schematic shown in Figure 5. In the circuit, the input terminal A refers to the enable input and B refers the clock input. The proposed transmission gate based D flip-flop with clock gating schematic in tool is shown in Figure 14, which is the same as the circuit in Figure 9.

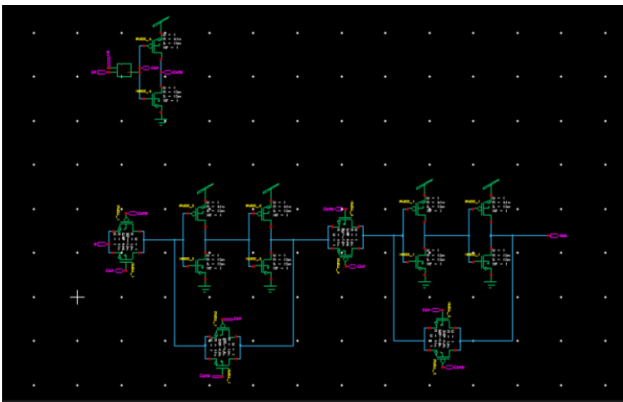


Figure 14. Schematic of proposed TG-based D flip-flop with clock gating in tool.

Figure 15 shows the output of the proposed transmission gate based D flip-flop with clock gating. Whenever the Enable and the Clock is in high

condition then only the output data are transferred otherwise the output remains in the same condition. This reduces power consumption. The first waveform shows the Enable input and the second one is the clock input. The gated clock input is shown in the third waveform. The D input and flip-flop outputs are shown in waveforms 4 and 5 respectively.

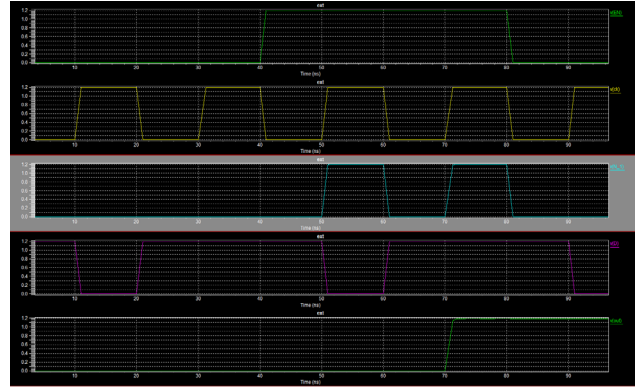


Figure 15. Output waveforms TG-based D flip-flop with clock gating in tool.

The inputs and obtained output values are given below.

Enable:	0 0 0 0 1 1 1 1 0 0 (input)
Clk:	0 1 0 1 0 1 0 1 0 1 (input)
gated clock:	0 0 0 0 0 1 0 1 0 0 (output based on clock gating)
D input:	1 0 1 1 1 0 1 1 1 0 (input)
Vout:	0 0 0 0 0 0 0 1 1 1 (flip-flop output)

The flip-flop output is zero for the first five D inputs, since the gated clock is zero. The output remains in its previous condition (0 value). Next gated clock becomes 1 and the D value is 0 and is stored in the flip-flop (output becomes 0). It is maintained until the gated clock becomes 1. The gated clock becomes 1, the D input is also 1 (8th bit), the flip-flop output changes to 1.

Figure 16 shows the serial in parallel out shift register using the proposed D flip-flop with clock gating. The register accepts serial input (one bit at a time through a single data line) and generates parallel output. The circuit consists of three connected D flip-flops^[21]. All three of the flip flops are coupled with the clock signal and the enable signal and D input signal. The first flip-flop output is given to the

second flip-flop as D input and so on. All the flip-flop receives the same clock signal and is having a clock gated module. The gated logic circuit allows gated clock only whenever there is a change in input value.

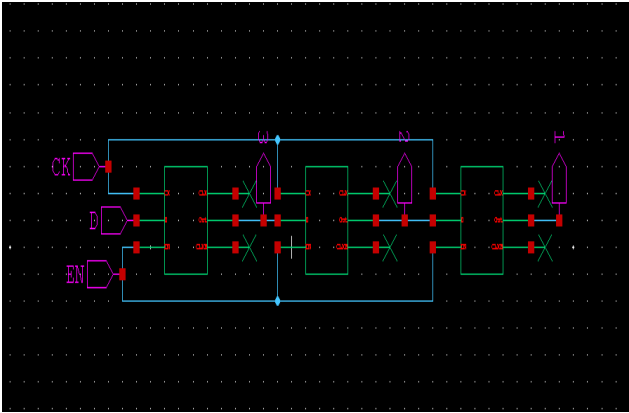


Figure 16. Serial-in parallel-out shift register in tool.

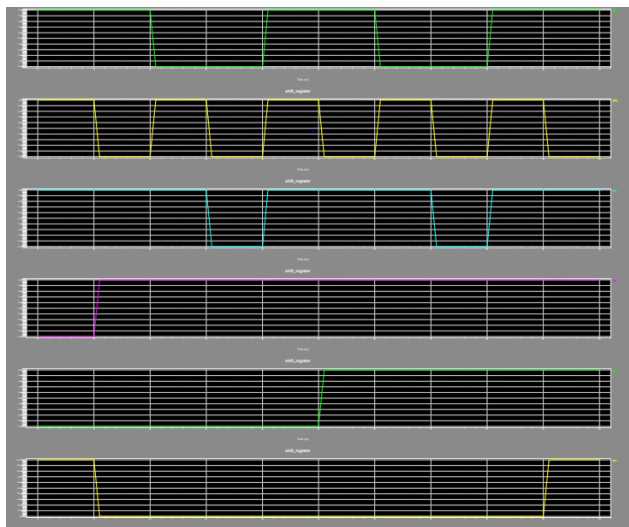


Figure 17. Output waveforms of the shift register in tool.

Figure 17 shows the output of the three-bit shift register and five clock pulses are applied to the circuit to store the data ‘1 1 1’. The gated pulse triggering circuit (clock gating) allows only three pulses to the flip-flop. These pulses are used to move and store the given input D values in the shift register. This avoids unnecessary switching of transistors in the circuit and saves power.

The power consumption of the proposed D flip-flop with clock gating is less when compared to the existing transmission gate based flip-flops and is given in Table 1.

Table 1. Comparison of proposed work and existing work.

Method	Power	Number of transistors	Delay
Transmission gate-based D flip-flop without clock gating (Conventional)	0.24 mW	24	20.02 ns
Transmission gate based D flip-flop with clock gating	0.17 mW	30	10.23 ns
Modified Transmission gate-based D flip-flop without clock gating	4.699 μ W	18	60.02 ns
Modified Transmission gate-based D flip-flop with clock gating (Proposed work)	3.092 μ W	24	49.16 ns

6. Conclusions

In this paper, a clock gated pulsed D flip-flop using a transmission gate was implemented. The gated clock reduces the unnecessary switching of the transistors in synchronous circuits and in turn, the dynamic power consumption of the circuit is also reduced. First, the clock gating circuit was implemented. Next, the transmission gate-based D flip-flop, modified transmission gate-based D flip-flop performances are measured with and without clock gating. The performances are analyzed in terms of power, the number of transistors and delay. The power reduction of 1.586 μ W (34%) was achieved using the clock-gated modified transmission gate-based D flip-flop when compared to the without clock gating condition of the same circuit. The delay is more in the proposed circuit, since the gated clock circuit increases the delay. A 3-bit serial-in and parallel-out shift register was also constructed using the proposed D flip-flop and its average power was 4.22 μ W watts which is less than the conventional 3-bit shift register without clock gating. The proposed design pulsed D flip-flop is useful for low power applications.

Conflict of Interest

There is no conflict of interest.

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