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ARTICLE

A Novel Process for SiGe Core-Shell JAM Transistors Fabrication and Thermal Annealing Effect on Its Electrical Performance

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ABSTRACT

In this study, we fabricate Si/SiGe core-shell Junctionless accumulation mode (JAM)FinFET devices through a rapid and novel process with four main steps, i.e. e-beam lithography definition, sputter deposition, alloy combination annealing, and chemical solution etching. The height of Si core is 30 nm and the thickness of Si/SiGe core-shell is about 2 nm. After finishing the fabrication of devices, we widely studied the electrical characteristics of poly Si/SiGe core-shell JAM FinFET transistors from a view of different Lg and Wch. A poly-Si/SiGe core -shell JAMFETs was successfully demonstrated and it also exhibits a superior subthreshold swing of 81mV/dec and high on/off ratio > 10^5 when annealing for 1hr at 600°C. The thermal diffusion process condition for this study are 1hr at 600°C and 6hr at 700°C for comparison. The annealing condition at 700oC for 6 hours shows undesired electrical characteristics against the other. Results suggests that from over thermal budget causes a plenty of Ge to precipitate against to form SiGe thin film. Annealing JAMFETs at low temperature shows outstanding Subthreshold swing and better swing condition when compared to its counterpart i.e. at higher temperature. This new process can still fabricate a comparable performance to classical planar FinFET in driving current.

1. Introduction

Complementary metal-oxide-semiconductor (CMOS) device have been the dominant device for ultra large -scale integration (ULSI) in semiconductor industry for decades due to its high speed and low power consumption. In recent years, owing to the limitation in miniaturization of VLSIs, we are looking for a novel material introduction to replace the planar Si channel devices in order to achieve high performance. Alternate channel materials such as Ge and SiGe are in great interest due to their higher mobility than Si. Moreover, stereoscopic channel structure are the primary methods to advance performance.

Si/SiGe core-shell hetero-structures are recognized as the most promising solutions to further continue the Moore's law beyond conventional planar bulk technologies are in great interest for p-type high-performance MOSFET. Core/shell structures with either Si or Ge as the core or shell have been researched such as Ge/Si [1], SiGe/Si [2], or Si/Ge [3] core/shell NW hetero-structures have been proposed to improve the hole transport in p-type FETs. Compared to traditional 2D Si planar devices, core-shell hetero-structure devices offer higher drive current

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and strong gate controllability due to its geometrical advantage. A core-shell MOSFET fabrication approach passes through two-step process. First, grow core structure through bottom-up [2-4] or top-down [1,5] methods. Second, the shell structure around the core is grown by chemical vapor deposition (CVD). However, there exist a challenge in this method that hetero-epitaxy is very difficult in the case of horizontal layers [6].

In this study, we fabricate core-shell devices through a rapid and novel process with four steps, i.e. e-beam lithography definition, sputter deposition, alloy combination annealing, and chemical solution etching. Different from above methods, we introduce a whole low cost and low thermal budget methods for core-shell structure fabrication a new choice.with the miniaturization of the channel length, the diffusion problem of short-channel junction doping occurs and it is difficult to accurately control the abrupt junctions [7]. Thus, the junctionless (JL) FETs have been proposed to solve the problem in the fabrication of ultra-shallow and abrupt junctions profile [8-10]. Different from inversion-mode (IM) FETs, because channel and S/D of junctionless (JL) FETs have the same heavily doping concentration and doping types, there is no PN junctions exists between channel and S/D. Furthermore, (JL) FETs have different conduction mechanism compared to the inversion-mode (IM) FETs.

Figure 1 shows the cross-sectional structures of p-type FETs along the S/D direction showing the doping profile, including (a) inversion mode (IM) FETs, (b) junctionless (JL) FETs [9,10]. Owing to thermal diffusion of S/D dopants into the channel, (IM) FETs has a shorter effective channel length than the physical channel length. For the (JL) FETs, because the work function difference between the gate electrode and the channel pushes away the depletion region from gate edge to the S/D, it has a longer effective channel length than the physical channel length [11]. Hence, (JL) FETs are regarded as having stronger immunity against short-channel effects than (IM) FETs [12-14].Because of the large number of carriers, there is a big challenge in the (JL) FETs process that carriers in the channel are difficultly fully depleted. For this reason, the channel dimension of (JL) FETs must be a small cross-sectional area. However, (JL) FETs have a critical issue which is high S/D parasitic resistance due to the small channel dimension and random dopant fluctuation (RDF) [15]. To overcome these problems, junctionless accumulation mode (JAM) FETs have been proposed. Junctionless accumulation mode (JAM) FET with additional S/D implantation have been implemented for lowering the S/D parasitic resistance [9,16,17], as shown in Figure 2. Different from conduction mechanism of (JL) FETs, when devices turn on, (JAM) FETs have an accumulation layer at the channels surface [9].

In this study, we proposed a (JAM) FETs but without channel doping, the SiGe channel is intrinsic. And we depend S/D implantation with B^{11+} to demonstrate a p-type junctionless accumulation mode FETs. After introducing several concepts above, we can briefly clarify the target to effectively achieve novel way of process for fabricating SiGe Core-Shell transistors.

2. Experimental Procedure

In this study, we demonstrate a Si core cladded with a SiGe shell JAMFET, there are several methods to fabricate Si core / SiGe shell structure, such as SiGe condensation [6,18] or directly epitaxy SiGe layer on the Si fins [19]. Here, we choose DC sputter to deposit Ge on the Si fins. The reason why we choose sputter deposition to fabricate core-shell is that sputtering has advantages such as high purity and vacuum, furthermore, it can form a thin film in low temperature.

Main process flow is shown in Figure 3. Device fabrication begins on a 6-inch Si wafer grown with 200 nm wet oxide, after that, a 50-nm-thick Si_3N_4 layer is deposited on it. Then the 40-nm-thick undoped amorphous Si (α-Si) layer is deposited via low-pressure chemical vapor deposition (LPCVD), then α-Si is transformed to poly-Si through solid-phase crystallization (SPC) for 24 hrs at 600°C in N_2 ambient.

The active region is defined by E-beam stepper and reactive-ion etching (RIE) to form a poly-Si fin-channel. Then, 12-nm-thick amorphous Ge (α-Ge) layer is deposited by sputter and 20-nm-thick PESiO_2 is deposited on amorphous Ge layer to prevent Ge from oxidation during the thermal process. The combination of amorphous Ge between poly-Si is via the horizontal furnace tube in different annealing temperature and time i.e. 1 hr at 600°C and 6 hr at 700°C to form the different Ge content in SiGe channel. However, the Ge completely covers whole wafer during sputtering. Because the etching selective ratio between SiGe and Ge is different, we depend on wet etching method to remove the residual Ge on the Si_3N_4 layer. We choose the etching solution from a few papers[20,21] and the suitable choice is ($HCl+H_2O_2$) : H_2O 0.5% at the room temperature. As mentioned in process flow, the poly-Si core/poly-SiGe shell structure channel is fabricated. Next, the gate oxide of 7-nm-thick Al_2O_3 is deposited by ALD and the TiN is deposited immediately as gate metal. After the gate patterning, B^{11+} implantation (1×10^{15} cm^{-2} at 10 keV) was carried out to form p-type S/D and the dopant activation is done through microwave annealing and the schematic configurations of key process steps for the po-

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ly-Si / SiGe core-shell JAMFETs are shown in Figure 4. Finally, material and electrical performance of poly-Si/ SiGe JAMFET were analyzed and discussed for two thermal annealing condition i.e. 1 hr at 600°C and 6 hr at 700°C.

3. Results and discussion

Figure 5 shows the depth profile of active region after the SiGe combination annealing by the X-ray photoelectron spectroscopy. As shown in Figure 5, the SiGe shell composition can be observed, the content of Ge at the channel surface are 20.8%,36.4% and 32.9% for different annealing condition (1hr at 600°C,1hr at 700°C and 6hrs at 700°C), respectively. In addition, no matter which annealing condition is, the profile of Ge has higher content at the surface forming a SiGe alloy. When etching depth reaches a deeper position, the Ge content decrease obviously about below 5%. In this paper, we will mainly perform observe electrical performance at annealing condition for 1hr at 600°C and 6hrs at 700°C It is noteworthy that when the annealing temperature is 700°C, more Ge penetrating into the Si layer than annealing temperature is 600°C. Hence, the Ge penetration is severe for higher annealing temperature. Finally, SiGe is detected on the shell of this structure through energy dispersive spectrometer (EDS). From Figure 6 we can demonstrate that the element content on the shell of silicon and germanium is 85.35% and 14.65%.

In this part, we investigate the material analysis results and electrical parameters of poly-Si /SiGe core-shell JAMFETs with different SiGe combination annealing conditions. The measured dimensions of channel width (W_{ch}) are 40 nm,60 nm,80 nm and 100 nm and gate length (L_g) are 60 nm,80 nm,100 nm,120 nm,150 nm,200 nm and 400 nm. Figure 7 shows the cross-sectional transmission electron microscope (TEM) image of poly-Si/SiGe core-shell JAMFET. In Figure 7, a rectangular shape core-shell structure is successfully fabricated in which channel width (W_{ch}) × channel height (H_{ch}) is (68 × 30)nm and effective width (W_{eff}) is 128 nm. We observe that the white region is a 2.17 nm-thick thin SiGe layer cladding on a 30 nm-thick poly Si layer after chemical solution etching and a 5.16 nm-thick Al_2O_3 layer and a 63.25 nm-thick TiN surround the core-shell channel.

We expect that the specific condition of annealing can combine Ge and Si at the channel surface but rarely penetrates Ge into Si. There are mainly two SiGe combination annealing condition i.e. 1hr at 600° and 6hrs at 700°C in N_2 ambient. The sample structure is poly $Si_{1-x}Ge_x$ (x = 20% ~ 37%) / poly Si / wet SiO_2 / substrate. Furthermore, we investigate the electrical characteristics such as I_D versus V_G, threshold voltage, subthreshold swing, DIBL and on current of the condition of Poly-Si /SiGe core-shell JAMFETs when SiGe combination annealing condition is 1hr at 600°C and 6hrs at 700°C with different dimension. The electrical performance of poly-Si/SiGe core- shell JAMFETs were measured at room temperature by semiconductor device analyzer (KEITHLEY, version V9.1 SP3). Figure 8 shows the outstanding transfer characteristics of poly-Si/SiGe core -shell JAMFET with channel width =40nm and gate length of 100nm for different annealing activation time. i.e. for 1hr at 600°C and 6hr at 700°C, respectively. The p-type Poly-Si / SiGe core-shell devices for 1hr annealing at 600°C perform a superior S.S. in comparison to the annealing for longer duration of annealing at 700°C and the resulting value is 81 mV/dec and 101 mV/dec, respectively and I_{ON}/I_{OFF} ratio is > 10^5. It indicates that there is improvement in sub-threshold swing when annealing for less annealing duration and temperature. Subthreshold swing was relatively higher in case of high annealing condition of Si/SiGe core shell JAMFET device. This may be due to the relatively higher interface trap density in SiGe channel when annealing at high temperature. Figure 9 displays the on-state current for p-type Poly-Si / SiGe core-shell JAMFETs as function of different channel width and fixed gate length=100nm, where gate voltage(Vg) was varied from 0 to -2.4V with a step of -0.6V. The resulting drain current is higher in case of annealing for 6hr at 700°C when compared to its counterpart i.e. annealing for 1hr at 600°C. In an ideal MOSFET, I_d is expected to be linearly dependent on V_{gs}, as shown by equation (1).

$$I_d = C_{ox}\mu\frac{W}{L}\left[\left(V_{gs}-V_t\right)V_{ds}-\frac{V_{ds}^2}{2}\right] \quad (1)$$

Where, I_d= Drain current, C_{ox}= Oxide capacitance.

To extract V_t, an often-used method is the transconductance method, where the improved transconductance g_m is given by:

$$gm = \frac{W}{L}\frac{2a}{q}C_{OX}^2\left(V_{gs}-V_t\right)V_{ds} \quad (2)$$

Where; α= common base current gain, q=magnitude of electron charge.

Figure 10 and Figure 11 shows I_D vs V_G characteristics of the poly-Si / SiGe core-shell JAMFET at various fin width and fixed gate length of 100nm for 1hr at 600°C and 6hr at 700°C. The figure shows that there is no strong dependence between on current as the channel

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width varies and the gate length except for that the minimum device of W_f= 60 nm demonstrating lower on current. By comparing the two figures, we know that the V_t roll-off phenomenon due to short channel effect is much more severe on the device for longer duration of thermal annealing condition. Furthermore, the sub-threshold properties and on-off current ratio are also degraded when the channel width increases. Figure 12 shows the distribution of subthreshold swing (SS) as function of gate length of 100nm and various channel width for 1hr at 600°C and 6hr at 700°C, respectively. It reveals that as the channel width increases from 40nm to 100nm ,the subthreshold swing also increases somewhat linearly. The minimum subthreshold swing was observed at channel width of 40nm for 1hr at 600°C and the maximum swing was observed at channel width of 100nm for 6hr at 700°C,indicating the degradation of gate controllability. Subthreshold swing remains almost constant and low in the annealing condition of 1hr at 600°C for channel width of 40nm and 60nm. In contrast, the electrical performance of neutral beam etched devices is similar within the gate length region of 150 ~ 400 nm, indicating better control of the interface properties. Figure 13 shows the dependence of threshold voltage a function of different gate length at a fixed fin width=60nm under two different annealing condition for poly-Si/SiGe core-shell JAMFETs. Figure 13(a) shows the short channel effect in terms of decreasing threshold value as it is annealed at low annealing duration for 600°Cfrom and the highest threshold voltage is about 0.299V at W_{ch} x L_g of 60 nm x 120 nm and the lowest threshold voltage is about -1.72V at W_{ch} x L_g of 60 nm x 200 nm.

From Figure 13(b), We observe that the rough trend of threshold voltage is decrease with gate length becoming long shows the short channel effects. The highest threshold voltage is about 1.53V at W_{ch} x L_g of 60 nm x 80 nm and the lowest threshold voltage is about -2.95V at W_{ch} x L_g of 60 nm x 400 nm. It is noticeable that the increase in gate length of channel material results in decrease on V_{th} of JAMFETs. Figure 14 shows the dependency of ON current on gate length of poly-Si/SiGe core-shell JAMFET at channel width of 40nm for 1hr at 600°C and 60nm for 6hr at 700°C, respectively. With the decrease in fin width, generally a slight increase in threshold voltage and a decrease in on current can be observed. In a thinner body, there are fewer amounts of inversion charge, and this is observed as a decrease in sub-threshold current and an increase in threshold voltage. With regards to the decrease in on current, it is directly related to the decrease in channel width, as can be referred in equation 1.For higher annealing temperature and longer duration ,On current slightly decreases with increase in gate length and the similar phenomena is observed for lower annealing temperature. From Figure 15 we can recognize that Ge is precipitated due to over thermal budget treatment in 6hrs 700°C annealing process. Our poly-Si/SiGe core-shell JAMFETS have shown quite good channel width scalability at low temperature thermal annealing when compared to longer annealing criterion. We realized a Si core cladded with a SiGe shell MOSFET which is fabricated with DC sputter to deposit Ge on the Si fins and through the horizontal furnace annealing in N_2 ambient and chemical etching process to remove residual Ge. In this study, driving current of silicon germanium for these devices is boosted. Although the V_{TH} displays there are still have SCE in these devices.

4. Conclusions

In this study we have demonstrated a Poly-Si /SiGe core-shell structure and investigated the electrical characteristics of Poly-Si /SiGe core-shell JAMFETs. The experimental results can be confirmed in the cross-sectional transmission electron microscope (TEM) image and energy dispersive spectrometer (EDS). A Poly-Si / SiGe core-shell gate stack is displayed in cross-sectional transmission electron microscope (TEM) image. There is a very thin SiGe layer cladding the Si fin forming a Si/ SiGe core-shell structure. The results of this study provide demonstration of novel technologies as well as physical insight into their performance. Studying in the terms of the electrical performance of Ion and S.S., we can observe that SiGe combination in the condition of 1hr 600°C precisely transfer and effectively enhance the electrical characteristics. The JAMFETs with channel width of 40nm and gate length of 100nm for 1hr at 600°C demonstrates the outstanding subthreshold swing of 81mV/dec and on/ off ratio $>10^5$. Compare to above results, the Ion of SiGe combination in the condition of 6hrs 700°C doesn't show the behavior which SiGe can strengthen the drive current. Also, the value of SS of SiGe combination in the condition of 6hrs 700°C is higher than previous conditions. Furthermore, we introduced a whole low cost and low thermal budget methods for core-shell structure fabrication as a new option.

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Appendixes

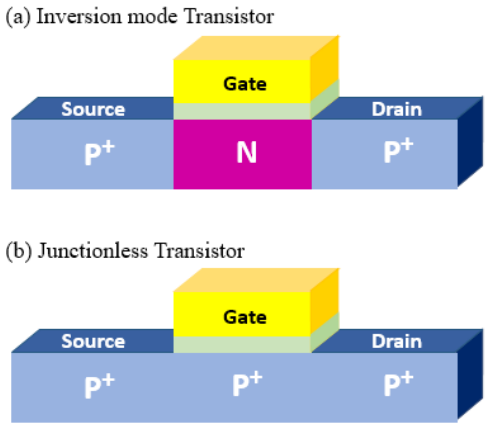

Figure 1. Cross-sectional structures of p-type FETs along the S/D direction (a) inversion mode (IM) FETs, (b) junctionless (JL) FETs

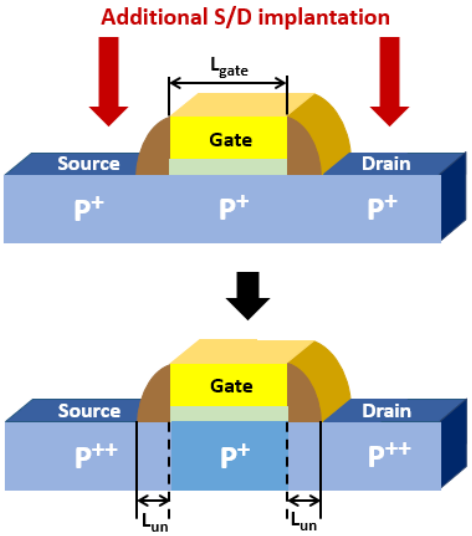

Figure 2. Junctionless (JAM) FET with additional S/D implantation

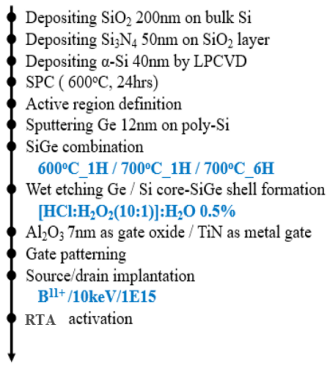

Figure 3. Process flow of the poly-Si / SiGe core-shell JAMFETs

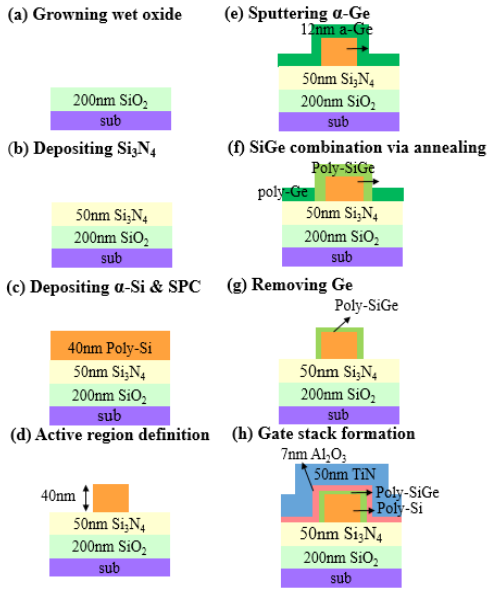

Figure 4. Schematic configurations of key process steps for the poly-Si / SiGe core-shell JAMFETs

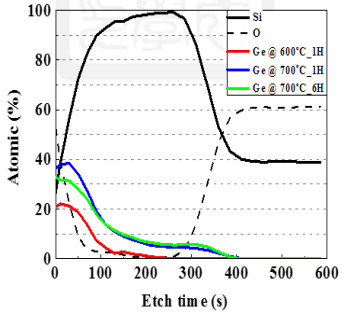

Figure 5. The depth profile of active region with three SiGe combination annealing condition,i.e.600°C_1hr,700°C_1hr,700°C_6hr

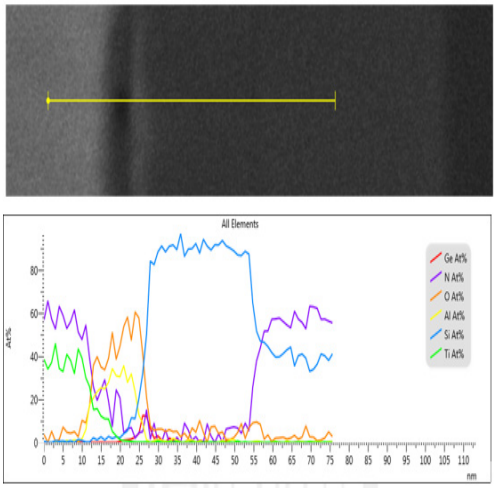

Figure 6. The element content distribution of poly-Si / SiGe core-shell JAMFETs by energy dispersive spectrometer

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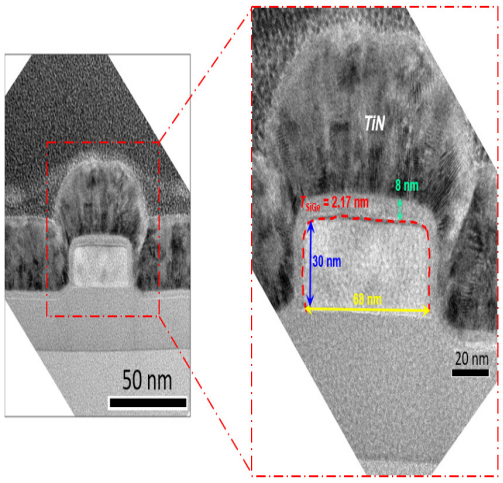

Figure 7. Cross-sectional TEM image of poly-Si / SiGe core-shell JAMFETs along the gate (b) The enlarged TEM image with H_{ch} = 30 nm, W_{ch} = 68 nm

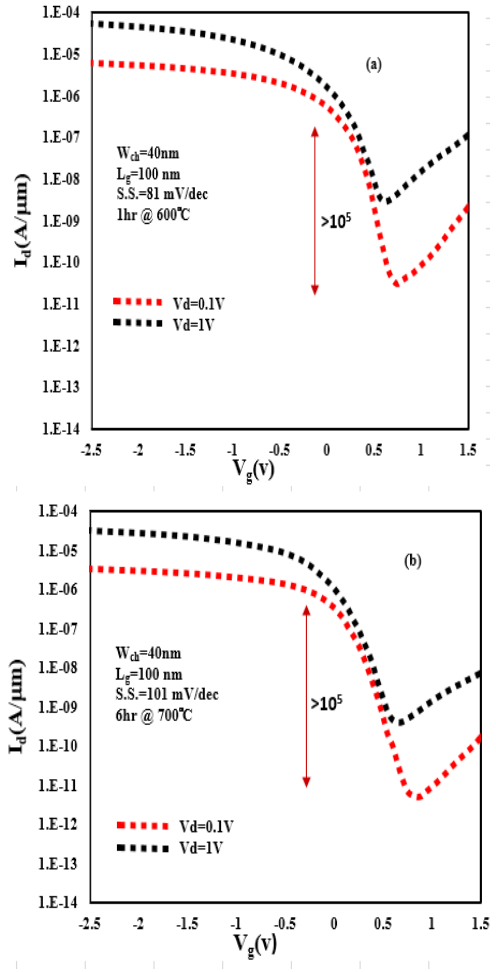

Figure 8. The outstanding transfer characteristics of the poly-Si / SiGe core-shell JAMFET at (a)Wch of 40 nm and Lg of 100 nm for 1hr at 600°C (b) Wch of 40 nm and Lg of 100 nm for 6hr at 700°C, respectively

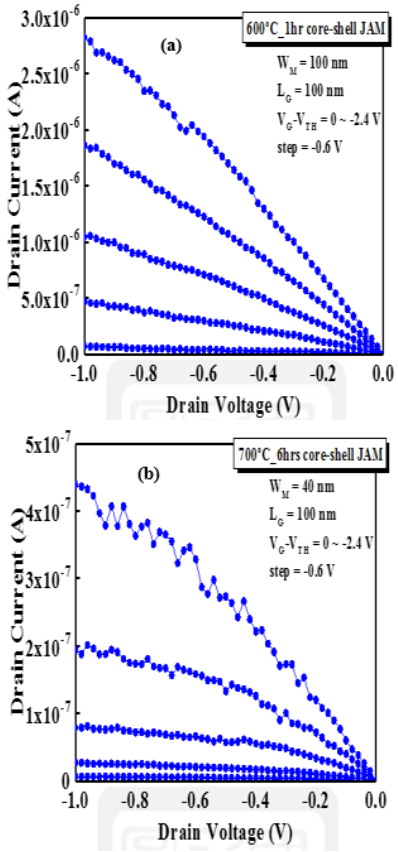

Figure 9. The outstanding I_D-V_D of the poly-Si / SiGe core-shell JAMFET at (a)W_{ch} of 100 nm and L_g of 100 nm for 1hr at 600°C (b) W_{ch} of 40 nm and L_g of 100 nm for 6hr at 700°C, respectively

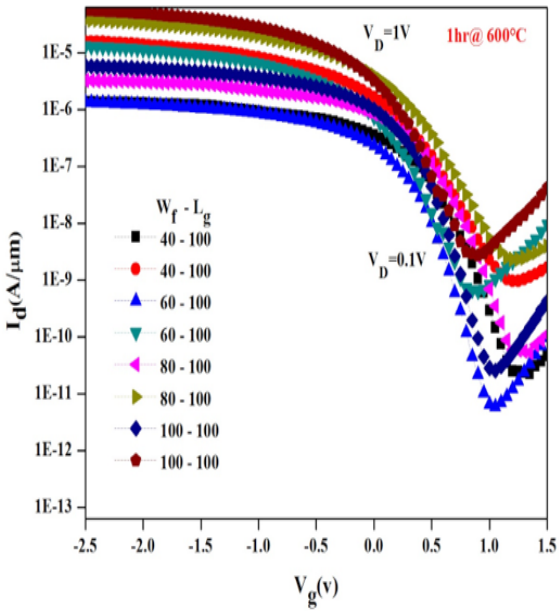

Figure 10. I_D vs V_G characteristics of the poly-Si / SiGe core-shell JAMFET at various fin width and fixed gate length of 100nm for 1hr at 600°C

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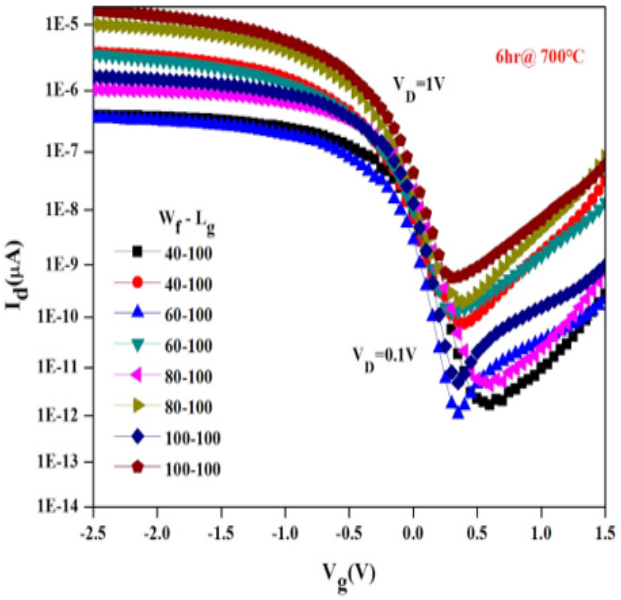

Figure 11. I_D vs V_G characteristics of the poly-Si / SiGe core-shell JAMFET at various channel width and fixed gate length of 100nm for 6hr at 700°C

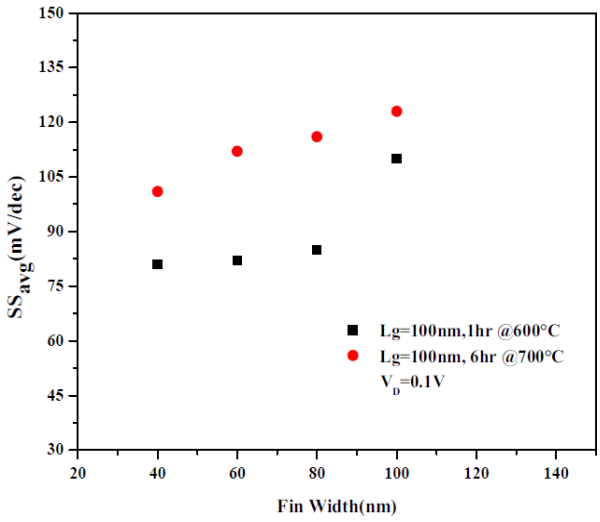

Figure 12. Distribution of subthreshold swing (SS) vs various channel width and fixed gate length of 100nm for 1hr at 600°C and 6hr at 700°C, respectively

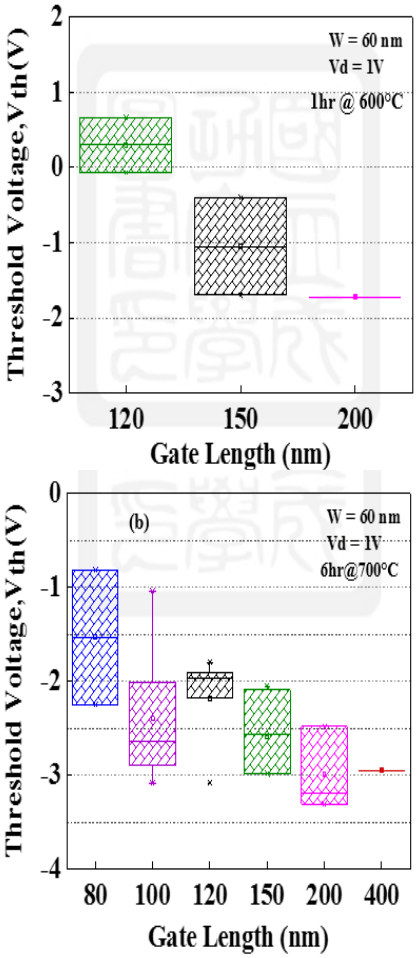

Figure 13. The comparison for statistic distributions of V_{th} for the poly-Si / SiGe core-shell JAMFETs at W_{ch} of 60 nm with different L_g for different annealing condition,(a) for 1hr at 600°C, (b) for 6hr at 700°C, respectively

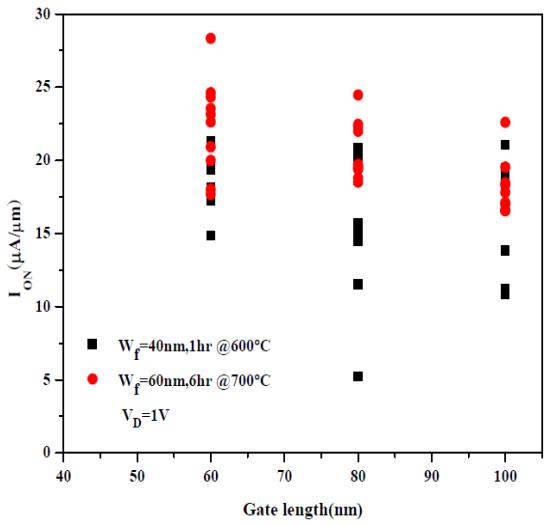

Figure 14. Dependency of ON current on gate length of poly-Si/SiGe core-shell JAMFET at channel width of 40nm for 1hr at 600°C and 60nm for 6hr at 700°C, respectively

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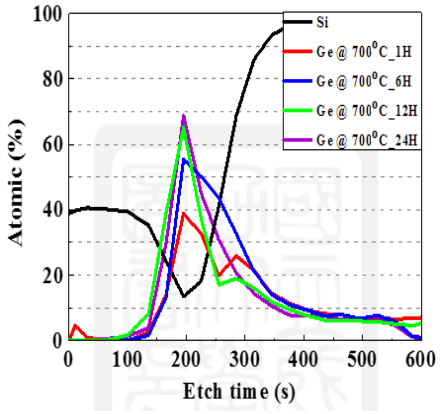

Figure 15. The depth profile of active region with four SiGe combination annealing condition,i.e.700°C_1hr,700°C,_6hrs, 700°C_12hrs and 700°C_24hrs

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