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ARTICLE

Flip Chip Die-to-Wafer Bonding Review: Gaps to High Volume Manufacturing

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ABSTRACT

Flip chip die-to-wafer bonding faces challenges for industry adoption due to a variety of technical gaps or process integration factors that are not fully developed to high volume manufacturing (HVM) maturity. In this paper, flip-chip and wire bonding are compared, then flip-chip bonding techniques are compared to examine advantages for scaling and speed. Specific recent 3-year trends in flip-chip die-to-wafer bonding are reviewed to address the key gaps and challenges to HVM adoption. Finally, some thoughts on the care needed by the packaging technology for successful HVM introduction are reviewed.

1. Introduction

Flip-chip die-to-wafer (D2W) bonding is gaining traction as a preferred small or chip-scale package (CSP) technique for chip packaging integration when technically superior or limiting as compared to wire bonding. Reviewing IEEE conference papers and TechInsights search engines for trends in the development and application of this packaging technique indicates that it has been increasing in applications over the last several years. It is well established that wire bonding continues to be the dominant die to packaging interface; however, as flip-chip D2W increases in applications, it will be natural to desire an understanding of the limits to high volume manufacturing adoption and ensure economic development scaled adoption are addressed.

This paper seeks to review the basis of flip-chip ver-

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sus wire bonding, examine the latest trends of flip-chip packaging with particular concern to D2W bonding and various gaps associated with D2W bonding technology. High volume manufacturing (HVM) adoption truly will rely on low defects and highly reliable and scalable methods. Even if the packaged device demands flip-chip D2W as the preferred interconnection between the chip and package, the technology will scale economically, with low yield losses to improve the ramping. A schematic of wirebonding and flip chip technology is shown in Figure 1.

We will begin by reviewing the basic advantages of flip-chip as compared to wire bonding. Then consider the typical flip-chip bonding techniques available, followed by a literature review to understand the latest trends. We focus on more recent literature which may be a lagging indicator that flip-chip bonding has focused on D2W applications utilizing hybrid bonding techniques. Furthering the literature review of flip-chip and wire bonding, we will review several process/technology gaps that are highlighted and then consider how these gaps could drive a robust HVM adoption strategy.

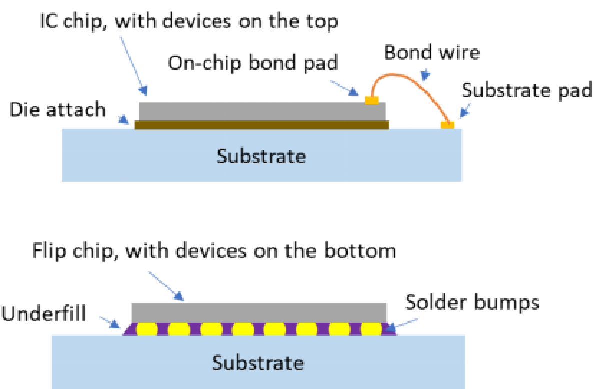

Figure 1. Schematic of wirebonding (top) and flip chip (bottom) technology

2. Flip Chip Die-to-Wafer Bonding

2.1 Advantages of Flip Chip vs. Wire Bonding

It is well established that the majority of the semiconductor chip-to-package interconnections are implemented through wire bonding technology, therefore, we should consider carefully the advantages of wire bonding to flip-chip bonding to appreciate the reasons for adoption in advance of reviewing the recent trends in flip-chip packaging. Flip-chip packaging was introduced as early as 1969 by IBM [1], yet it continues to enjoy a very minor portion of interconnect bonding application. So, despite very limited adoption of this technique for chip-to-package interconnection, we should make a brief review of the advantages of both wire bonding and flip-chip packaging, as shown in Table 1 [2].

Table 1. Wirebonding and flip-chip comparison

Wire Bonding	Flip-Chip
Higher flexibility	Higher device Speed
Mature infrastructure	Power and ground distribution
Lower cost	Higher I/O density with area array
High reliability	Lower package size/form factor
	Low stress over active area

The key advantages noted for flip chip to wire bonding are device speed, I/O density, and package size. CSP's intention to bring interconnection to the same size as the chip drives a need for more density in I/O (input/output) connections. Naturally lower parasitics or improved speed are also a benefit that package designer may take advantage of when selecting flip chip over wire bonding.

2.2 Flip-Chip Chip-Scale Package (CSP) Bonding

The flip-chip bonding for D2W includes solder ball with underfill (Figure 2 [3]), bump-bump underfill, TSV underfill, and Cu-Cu underfills and up to hybrid bonding, including thermal compression bonding (TCB) which bonds simultaneously both the bumps and underfill material using force and heat (Figure 3 [4]).

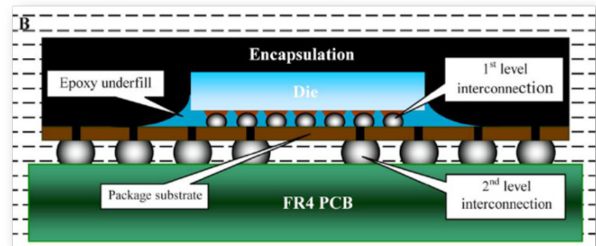

Figure 2. Flip chip bonding with solder ball and epoxy underfill

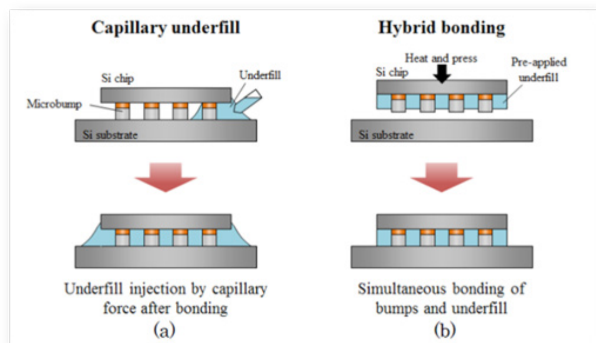

Figure 3. Flip chip bonding with underfill and hybrid bonding

Solder-based bonding allows pad pitches down to around 40 µm; whereas the underfill and hybrid bonding techniques are driving the I/O pitches down to about 10 µm and are projected to go even lower into nanometer scale as CSP scaling matches chip scaling for high-end fabrication. Next, we will make a brief review of the literature trends that support this observation.

2.3 Literature Trends as Lagging Indicator of Flip Chip Die-to-Wafer (D2W) Adoption

To gauge the adoption of flip-chip bonding, a review of all IEEE conference papers was conducted to cover the period of 2006-2021 [5]. Whereas, compared to wire-bonding in the same period, it was found that around 3,553 papers were issued compared to only 140 articles discussing flip-chip D2W [6]. Clearly, wire-bonding continues to dominate the literature.

To appreciate the trending of the flip chip papers a graph is shown in Figure 4 indicating some bimodality with a peak around 2009, a dip in 2012, but since then a steady increase in the number and persistence of papers issued to reach cumulative of 140.

To reduce the paper review to examine a more specific topic within flip-chip bonding, the papers issued in the last three years were sampled to find that hybrid bonding and D2W seem to be of particular importance for enablement of further I/O scaling, performance, and penetration into HVM scalable packaging. However, a key point of many of these papers is to uncover limitations, challenge, or gaps for adoption of the D2W bonding. Thus, we will next review some of the gaps highlighted as a consideration of issues that should be addressed to HVM adoption.

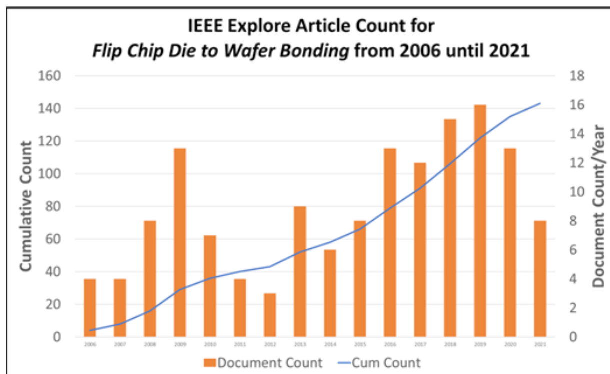

Figure 4. Flip chip conference papers in IEEE Explore, 2006-2021

3. D2W Bonding Gaps to HVM Adoption

High volume manufacturing (HVM) adoption will require a careful consideration of several technology gaps to allow successful scaling at cost, even in presence of a must-have technical application. A few key gaps are considered as follows.

3.1 Misalignment

Podpod et al. of Interuniversity Microelectronics Centre (IMEC) in Belgium discussed the path to scale D2W alignment to sub 2 µm tolerances as further means of scaling the D2W flip chip technology. In much of the literature, the common limit of nominal bonding machines was 3 µm [7].

The key cause discussed for the misalignment is the application of picking and placing known good die (KGD) from sample product to bond out to bottom wafer substrate. The solution discussed is to place the KGD into a preset carrier wafer system wherein an established grid captures a predetermined alignment; thus, the carrier wafer will reduce the alignment tolerance of individual pick and place technology to a common grid. This solution seems robust as it can achieve tighter tolerance than the prior art. It is likely that further D2W scaling will require tighter and tighter alignment tolerance due to diversity and size of chips and to allow further bump size reductions as well.

3.2 Wafer Warpage/Shape Issues

Podpod and the IMEC team also discussed the contribution of misalignment from vertical displacement due to wafer warpage. As the bottom wafer has been background or even due to the carrier substrate stresses, any warpage that may exceed ~ 200 µm was considered as a limit to permit successful bonding. Not only is a vertical misalignment problematic to the grid-to-grid match of carrier and bottom wafer, moreover, the underfill and TCB process need to maintain a small gap to ensure complete contact of all bonded surfaces [7].

3.3 Wafer Stress/Cracking

As fab's back-end-of-line (BEOL) process integrates low-k dielectrics while through-silicon vias (TSV) are included to facilitate flip-chip bonding methods, Shengmin and team at Synaptics discuss the problematic stress-cracking that may occur due to the combination of TSV in presence of the low-k dielectrics and propose modeling techniques to predict fail mode and allow designer to introduce yield enhanced layout [8]. Figure 5 below shows the complexity of Cu TSV and bumps in both 2.5D and 3D interconnect schemes that can lead to the various possible failure potentials that a designer may be interested in modeling.

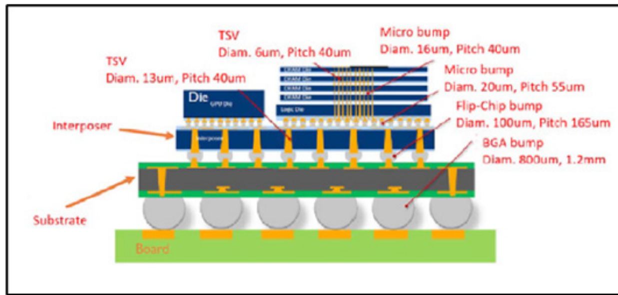

Figure 5. 2.5D/3D Heterogeneous Integration [8]

A key takeaway from Shengmin's work is the benefit for stress-crack reductions when design-aware layouts are introduced before the packaging layouts are confirmed and take on unknown risks to yield loss in the absence of modeling.

3.4 Die Mapping/Known Good Die (KGD)

Jean-Charles Souriau and the team at the University of Grenoble discuss the limitation of ultra-thin fan-out wafer level packaging to depend on the selection of KGD [9]. Although this paper's chief concern is to discuss the specific application of ultra-thin die in applications like wearable devices or folding devices, it does point to the HVM adoption concern to utilize yielding die in the D2W bonding technique. Since KGD must be picked from previously processed and background wafers, the added processing to select KGD is nearly offsetting the utilization of technique like wafer-to-wafer (W2W) bonding in which all fab yield maps will lead to failed package level product.

Further work to improve the preparation of KGD or to reach higher mature yields in fab will contribute to the development of further improved D2W vs W2W bonding and packaging techniques. In perspective as discussed here for ulta-thin device; it seems likely that non-heterogeneous 2D or 2.5D package will benefit from pre-selected KGD, whereas heterogeneous stacked products utilizing the same sized chips (like stacked memory) in a 3D package will benefit more from a W2W approach.

3.5 Cu CMP Uniformity

In applying D2W using Cu-Cu pads or vias, the formation of the connection will depend on the Cu CMP process to form the Cu pillar planarity with the surrounding dielectric. Guilian Gao and the team at Xperi describe the importance of CMP uniformity to create slightly recessed and isolated bond pads to enable HVM throughput D2W bonding when bonding alignment accuracy is near 3 µm [10]. Although no figures or graphs demonstrate the problems of poor CMP uniformity may present to D2W bonding, it is reasonable to expect that a uniform pad at dielectric level will couple with the underfill material along with bonding misalignment to further reduce the total cross-sectional area that is successfully bonded. Not discussed is any roadmap or scaling consideration of a) TSV or Cu Pillar size, b) bonding machine alignment tolerance, and c) CMP recess uniformity or d) alternate approaches to creating uniform substrate to pad-like dry etching with an overfill technique. Further study and modeling of the surface uniformity factors deserves additional work to improve roadmap scaling prediction; or the work to improve bonding machine alignment accuracy may be lacking.

3.6 Low Temperature Anneal

High-performance DRAM CMOS will not tolerate high differential temperature (DT) above as little as 250 °C [11]. Further, Gao (Xperi) and the team address DT. For anneal up to or exceeding 350 °C, issues may lead to surface oxidation and recombination of Cu pad leading to additional process yield concerns [11]. Thus, in a short review of literature, we can quickly appreciate that D2W bonding for HVM adoption will need to concern with a variety of DT limitations from the native DT limit a particular chipset may impose and up to the material behaviors at the bonding interface itself. Naturally, the DT limit will be enabled by selecting bonding materials for the back-end process that are stable at similar DT. Further, that anneal ramp study should be conducted to examine the transient heating effects on the critical interface. Not discussed is the need to conduct device electrical verification post D2W attach confirming performance is preserved. Additional testing will add cost and detract from D2W bonding method unless addressed.

3.7 Via Metallization for Reduced Parasitics

D2W TCB or Hybrid bonding may include the treatment of the metal selection for the bumps or pillars. Many of the reviewed literature discussed exclusively the use of Cu (likely due to fab BEOL friendly materials), but other authors have noted that pillars can be composite stacks including Cobalt, Tin, and Nickel [12]. Naturally, the utilization of the different stacks will feedback to the prior discussion on the DT limits as utilizing different materials can enhance the connection performance when faced with lot temp anneal or to address interface integrity based on faster anneal ramp for preferred connection in the TCB or Hybrid bonding technique. Fumihiro Inoue and the team at IMEC have explained that Co-Sn intermetallic pillars, when utilized in the D2W bonding requiring low DT anneals, are able to demonstrate improved connection due to the hybrid-metallic kinetics leading to higher yield

inter-metallic bonding at pad interfaces post bonding [12]. Although most conference papers discuss more often the use of Cu pillar or bumps, it is clear from this paper that one must consider the utilization of other metallics for improved physical bonds and improved yields. Further discussion and study of the different metallics for both direct performance improvement, low DT fitment, and fab BEOL process integration, should be explored.

3.8 Wafer Thickness Considerations

Jean-Charles Souriau and colleagues in the discussion of ultra-thin fan out wafer level D2W packaging also touched on the importance to control wafer thickness; and thus interconnection height as impacting to improved electrical performance [9]. While intended to meet the rigor of thin wearable products, thinner substrates also highlight that the lossless transmission line parasitics concerned with a longer line and thicker substrate are far improved in this specific application. Thus, one must consider other D2W packages if additional wafer thinning will be explored to improve the electrical performance and reduce the wafer warpage problem when the use of carrier wafers could be introduced. Not all performance requirements will be cost-justified, so the further development of this gap or capability may become increasingly important as the fabricator seeks to ramp effective solutions at cost.

4. Conclusions and HVM Adoption Recommendations

In this paper, we have considered that, for D2W bonding, a few bonding techniques are available to the packaging integrator, from solder ball to underfill TCB and hybrid bonding. A variety of specific application gaps and technology vectors are discussed to highlight that HVM adoption is not turn-key at this point while the technology appears to be very young as compared to the ever-dominant and mature wire bonding. As specific form-factor package size or device application for performance demand the foundry packaging firm or large-scale semiconductor fabricator who uses in-house packaging process, the adoption of the young technology begs careful planning to address the potential gaps and barriers to cost-effective, high yield, and scalable technology. I/O density will be limited by key factors like the bonding alignment accuracy, the pad or bump size and metallic interface, wafer or carrier wafer shape/warpage, interface uniformity if CMP technique has been utilized, anneal and DT limitation, underfill properties, bump metallic selection, stress induced crack formation; other gaps and risk not considered here must be carefully navigated to ensure the packaging design and process integration yield at device performance without degradation and providing low-cost and high-throughput solution. Nominally BEOL and even packaging technology is often under pressure to produce extremely low defect per million yield loss to ensure near 100% of packaged devices will be sellable units on account of fabrication of microchips are often faced with yielding constraints. The D2W integration is thus a dominant approach since it will allow the freedom of selecting KGD and avoiding yield losses that will increase at W2W packaging.

Based on the recent uptick in conference papers as well as the emergence of new suppliers and growth of the supply chain for this technology, the author believes this segment of microelectronic packaging at chip scale may be on the verge of breakout growth both at industry as well as organically in cases of leading-edge manufacturers who will seek to protect innovation and maintain cost or technical advantage over their peers. It certainly will be an interesting topic and technology to revisit in time to see if the pendulum will ever swing away from wire bonding and towards flip-chip bonding in the future.

Conflict of Interest

There is no conflict of interest.

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