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Performance Evaluation of Junctionless Cylindrical Gate-All-Around FET for Low Power Applications

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ABSTRACT

The advent of device miniaturization techniques and the evolution of very deep submicron technology have led to the increased prominence of short channel effects (SCEs) in conventional transistors (CTs). Now, in the era of nano-engineering and nano-wires, current research is centered around a novel device known as the Junctionless Field Effect Transistor (JLFET), which incorporates gate-all-around engineering applications. Given the challenges associated with scaling transistor sizes, such as creating high-quality junctions and changing doping concentrations (~10^{19} cm^{-3}) over a 10 nm distance, JLFET emerges as a promising alternative to CTs. Notably, JLFET lacks junctions and doping concentration gradients. In this study, the authors have conducted a comprehensive analysis and performance evaluation of JLFET and CTs, specifically in the context of low-power applications. Various performance parameters of JLFET, including SS, DIBL, transconductance, output conductance, and I_{on}/I_{off}, have been assessed. The findings indicate that JLFET exhibits reduced susceptibility to SCEs compared to CTs and demonstrates exceptional current driving capability.

Keywords: Short channel effects; Drain-induced barrier lowering; Subthreshold slope; Gate-all-around junction less FET; Device simulation

1. Introduction

Transistor sizes have reached a point where they are very close to fundamental limits, and the process of scaling down devices is approaching its saturation point. Moore's Law has long been the guiding principle for reducing the feature size of planar semiconductor technology. However, in today's landscape,

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Moore's curve is leveling off, and conventional transistors (CTs) have become so small that reducing leakage currents and addressing short channel effects (SCEs) has become increasingly challenging. As a result, there is a growing need for non-conventional architectural solutions, such as SOI (Silicon on Insulator) MOS architecture, ultra-thin body designs, Double Gate MOSFET (DG-MOSFET), FinFET, Tunnel FET (TFET), and various Multi-gate MOSFET configurations. In cases where the gate length and the overall distance between junctions in advanced three-dimensional devices dip below the 10 nm threshold, the significance of high doping concentration gradients becomes paramount for creating high-quality junctions. This is where the Junctionless Field Effect Transistor (JLFET) emerges as a promising alternative and an emerging device to the traditional CT.

There has always been a never-ending demand of high speed and low power consumption devices in the market. The feature size or the physical dimension of MOSFET has been incessantly scaled down to meet the requirement in accordance with Moore's Law. These basic fundamental units of integrated circuits manufactured today are nearly 25 times faster and fit into an area that is 1% of the area previously occupied by these devices. The scaling of the MOSFET is limited by scaling rules which dictate that the total amount of power consumed in the unit area remains constant. Gordon Moore in 1965 observed that on a chip the number of transistors could be doubled annually in 12 months for at least 10 years. But in these ten years, it was observed that the doubling time varied from eighteen months to three years. Gradually, the number of transistors on a chip decreased and the size of transistors was reduced. Thus, the Moore's postulate came to be known as Moore's Law. It represents a transistor count plot with respect to time for different processors. Moore came to the conclusion that the transistor count doubled every two years. Due to decrement in feature size, the density of transistors in a chip was increased. As a result, more functionality could be implemented in a single chip. Semi-conductor industry provides solutions for the hindrances encountered in CMOS technology. High density and robust performance can be achieved with the help of scaling. As we know, memory chips and logic chips play a vital role in the VLSI industry. Memory chips are highly regular in nature and thus, complexity can be increased thoroughly. So, increasing the density of memory chips is the major challenging issue in the VLSI domain [1].

Moore's law is the guiding factor for scaling down of feature size of planar semiconductor technology. Moore's law is the deciding factor for scaling down of feature size of planar semiconductor technology. In today's scenario, Moore's curve is saturating and CTs are becoming so small that it is becoming increasingly difficult to overcome SCEs like sub-threshold slope, drain-induced barrier lowering, mobility issues, temperature dependence, hot electron conduction, variability, parasitic resistance, parasitic capacitance, reliability and breakdown phenomenon etc. and therefore researchers are moving to different technology node by the help of scaling. Scaling is defined as the coordinated change in structural and electrical parameters of MOSFET so as to occupy a lesser silicon area while retaining the same behaviour. In scaled technology, the CTs are becoming so small that it is becoming increasingly difficult to overcome short channel effects (SCEs) which are very detrimental in performance improvement and energy saving. Therefore, there is a need of other technology nodes of MOSFET [2].

With continuously scaling the device dimensions, the device enters in sub-micron region. In this region, the performance of the device degrades due to rising Short Channel Effects (SCEs) and Narrow Channel Effects (NCEs). Hence, reducing these effects has been the focus in MOSFET scaling to improve the device reliability and performance. The substrate engineering proves to be very promising in order to figure out the short channel effects of sub-micron MOSFETs. In previous research, the concept of Substrate Engineering, with the help of SOI MOSFET structure has discussed and simulation results for evaluating the performance of Partially Depleted SOI MOSFET (PDSOI) and Fully Depleted SOI

MOSFET (FDSOI) have analyzed. These results will be applied to compare and intuitively understand these devices. SOI resists short channel effects (leakage current, sub-threshold current etc.) with fewer complexities in the process. The characteristics of SOI are low power dissipation, small parasitic capacitances, parasitic resistances and lower delay. The simulation results for evaluating the performance of Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET have been provided. The short channel effects issues of conventional MOSFETs have been discussed and seen the need for PDSOI and FDSOI based devices. SOI devices possess less parasitic but suffer from self heating effects. PDSOI suffers from lower threshold voltage, kink effect and history effect while FDSOI has no such problems. An ideal sub-threshold swing is another advantage of FDSOI devices. Hence, SOI has wide application in nano-electronics and also performances of FDSOI devices are better as compared to PDSOI devices [3].

The Junctionless Field Effect Transistor (JLFET) represents an innovative departure from conventional transistor technology by eliminating the need for junctions and the associated doping concentration gradients. This absence of source/drain regions and extensions simplifies the fabrication process considerably, offering significant advantages. In JLFET, all switching phenomena and ON-OFF actions are solely controlled by the gate, with variations in doping density and silicon size playing a pivotal role. Unlike traditional transistors, JLFET relies on bulk conduction rather than surface channel conduction, typically falling within the range of 10^{19} to 10^{20} cm^{-3} within just a few nanometers. In the pursuit of overcoming short channel effects (SCEs), gate-all-around MOSFETs have proven to be highly effective due to their comprehensive control over the entire channel area, owing to the "all-around" concept. However, when employing rectangular gate-all-around MOSFETs, they are susceptible to corner effect issues. To address this challenge, our work introduces a novel cylindrical-shaped gate-all-around technique within the JLFET architecture [4].

2. Mathematical modelling of JLFET

The basic concepts and mathematical modelling based on the current transport mechanism of JLFET have been studied. Basically, the current transport mechanism in JLFET is based on both analytical and numerical methods. Analytical models are based on Boltzmann Statistics and closed form solution of Poisson's Equation which provides an analytical relationship between gate voltage and surface potential. Numerical models analyze the device behaviour including motion quantization, sub-band splitting, fermi statistics, quasi-ballistic transport, surface and channel orientation and band structure. Then, mathematical analysis of JLFET in accumulation mode has been utilized in the proposed work [4]. **Tables 1 and 2** have depicted the drain current equations with different bias conditions.

Table 1. Drain current equations in JLFET.

Bias	Drain Current
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} < V_{DSat1}$	$I_D = \frac{q\mu_{bN_D}}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}\left((V_{GS}-V_{po})^{n+1} - (V_{GS}-V_{DS}-V_{po})^{n+1}\right) + S_{min}V_{DS}\right)$
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} > V_{DSat1}$	$I_D = \frac{q\mu_{bN_D}}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}\left((V_{GS}-V_{po})^{n+1}\right) + S_{min}V_{DS}\right)$
$V_{GS} > V_{FB}$ $V_{DS} < V_{DSat2}$	$I_D = \frac{q\mu_{bN_D}}{L_{effb}}\ S_{max}C_{ox} + \frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}\left(V_{DS}(V_{GS}-V_{FB}) - \frac{1}{2}{V_{DS}}^2\right)$

Source: [4].

Table 2. Symbol used in **Table 1.**

Symbol	Value
V_{po0}	Linear pinch-off voltage at $V_D = 0V$
V_{po}	Pinch-off voltage $V_{po} = V_{po0} - \eta V_{DS}$
η	DIBL coefficient
W_{eff}	Channel perimeter
S	Neutral (non-depleted) cross section of the channel: $S = S_{min}$ when the surface is inverted and $S = S_{max}$ when the surface is accumulated.
V_{DSat1}	Drain Saturation Voltage for the neutral bulk channel $V_{DSat1} = \frac{V_{GS} - V_{p0o}}{1 - \eta}$
V_{DSat2}	Drain Saturation Voltage for the accumulation channel $V_{DSat2} = V_{GS} - V_{FB}$
L_{effb}	Effective length of the neutral bulk channel
L_{effacc}	Effective length of the accumulation channel
μ_{acc}	Accumulation mobilities
μ_b	Bulk mobilities

Source: [4].

3. Theoretical and simulation framework

In this study, we delved into fundamental concepts and mathematical modeling, focusing on current transport mechanisms in both Conventional Transistors (CTs) and non-conventional CTs. Our exploration encompassed both analytical and numerical methods to gain a comprehensive understanding of these mechanisms. The concepts and mathematical modelling based on the current transport mechanism of CT have been discussed for performance evaluation. Basically, the current transport mechanism in CT is based on both analytical and numerical methods.

Analytical models drew upon Boltzmann Statistics and Poisson's Equation, offering analytical relationships between surface potential and gate voltage. On the other hand, numerical models provided a deeper analysis of device behavior, incorporating factors such as band effects, sub-band splitting, quasi-ballistic carrier transport, motion quantization, and considerations of surface and channel orientation. For the optimization of JLFET characteristics, we employed device simulation utilizing the ATLAS Device Simulator within the SILVACO TCAD Tool. This simulation aimed to uncover the performance capabilities of JLFET.

Our research findings were enriched by insights from other researchers in the field. Gnani et al. explored quasi-ballistic transport in nano-wires using Boltzmann Transport Equation (BTE) solutions and provided analytical solutions for I-V characteristics in one-dimensional quantum transport simulations [5]. Other researchers investigated quasi-ballistic transport using the Schrödinger equation with open boundary conditions and electron scattering phenomena, exploring band structure effects and addressing SCEs [6]. Lenzi et al. employed a Monte Carlo approach combined with the Boltzmann equation to study the transport mechanism of silicon nano-wires, yielding valuable results related to potential profiles, mobility, electron scattering, and I-V characteristics [7]. Poli et al. undertook a full quantum treatment of Coulomb scattering in silicon nano-wires FETs, offering solutions to the 3D Poisson-Boltzmann equation by incorporating the non-equilibrium Green's

Function formalism [8]. Han et al. provided insights into the subthreshold slope, threshold voltage, and current (Ion) for fully depleted p-type Junctionless Gate-All-Around (JLGAA) nano-wires [9]. Baruah et al. introduced an innovative approach involving high-k spacer dielectrics using dual-material gates for double-gate JLFETs, achieving excellent agreement with SCEs and enhancing fringing effects through spacer integration [10].

The device structure of the JLFET stands out for its relative simplicity when compared to CTs. JLFET functions essentially as a resistor and doesn't require the intricate junction implant techniques that CTs do. JLFET closely resembles an accumulation-mode FET, lacking PN or N^+N or P^+P junctions altogether. In JLFET, the predominant current flow is attributed to bulk conduction. In the ON state, a substantial body current flows owing to the high doping concentration in the channel region. Conversely, in the OFF state, the current is effectively halted due to the depletion of charge carriers. One notable advantage of JLFET is its reliance on bulk carriers for conduction, which sets it apart from other CTs, often referred to as inversion mode devices, where conduction occurs within the inversion layer at the surface region [11].

4. Fabrication and manufacturing process of JLFET

The fabrication process of JLFET is very simple with respect to CT. Because JLFET just works like a resistor and has no junctions, so there is no need of junction implant techniques. Junction-less nano-wire transistors with gate length down to 50 nm have been fabricated by some fabrication laboratories. The gate oxide thickness is 5 nm and electron beam lithography has been used to pattern both the nano-wires and the gates. **Figure 1** explains the cross sectional TEM picture of JLFET showing the structure of the device [11] and **Figure 2** shows the cross-sectional transmission electron microscopy (TEM) picture of JLFET [12].

The n-channel devices have been doped using arsenic to a channel concentration of 5×10^{19} cm^{-3} and P^+ poly-silicon has been used as gate material [13–15]. Chi-Woo Lee et al. have fabricated junctionless devices made on standard SOI wafers and patterned with nano-wires using e-beam lithography [16]. A. Kamath et al. have fabricated Junctionless CMOS transistors with independent double gates using lithography free device fabrication. They have used Silicon Nitride using LPCVD process with a gate oxide thickness of 45 Å [17].

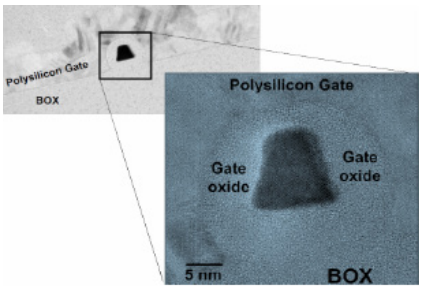

Figure 1. Cross sectional TEM picture of JLFET showing the structure of the device.

Source: [11].

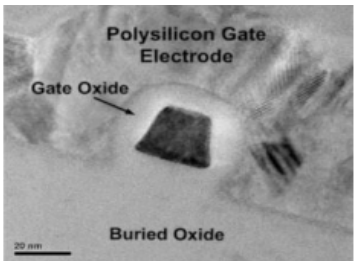

Figure 2. TEM cross section of a JLT nanowire transistor.

Source: [12].

5. Methodology

In our study, we conducted simulations of a cylindrical gate-all-around JLFET with a gate length scaled down to 30 nm and a radius of 10 nm with the study of International Technology Roadmap for Semiconductors (ITRS). A technology roadmap can help the researchers by giving an idea when a certain capability will be needed for a particular feature size and technology node. The geometrical settings and mesh design decision making process is crucial task. Many researchers have provided their results and we have provided new mesh design based results [15–19]. To perform these simulations, we utilized the SILVACO TCAD tools, running the entire script on ATLAS Device Simulator version: atlas 5.22.1.R, tailored for

the 30 nm technology node. The 3D coordinates for the cylindrical structure involved three regions: Silicon, SiO_2, and Poly Silicon, each characterized by its radius (in µm), angle (in degrees), and height (in µm). Within this design, we defined three electrodes: drain, source, and gate, each specified by its radius, angle, and height coordinates.

Of particular significance in this design was the use of the AUGUR model, which played a crucial role in accounting for recombination effects, especially relevant at high current densities. Solving semiconductor device problems necessitates the application of various numerical methods. In our case, we employed both the NEWTON and GUMMEL methods, addressing equations in both fully coupled and de-coupled forms. The n-channel devices were doped with arsenic to achieve a channel concentration of 10^{19} cm^{-3}. Additionally, P^+ poly-silicon, with a work function of 5.4 eV, served as the gate material. **Figures 3 and 4** provide visual representations of the device structure and net doping profile for the 3D JLFET, offering different viewing aspects for a comprehensive understanding.

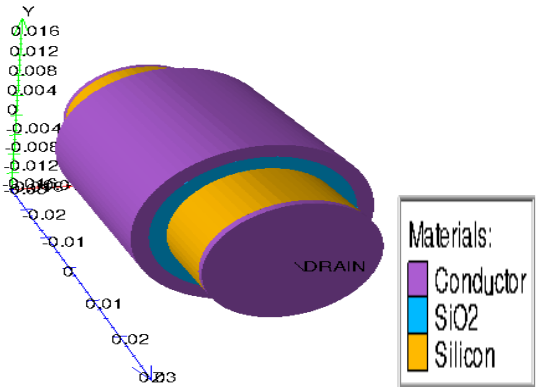

Figure 3. JLFET structure with solid view

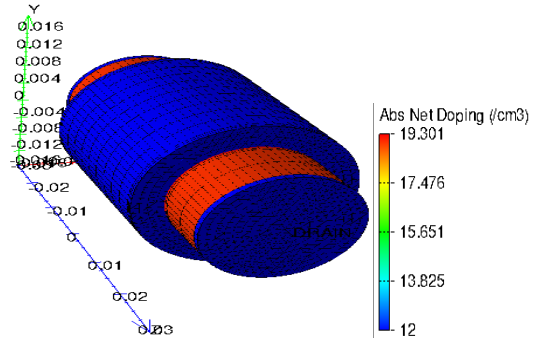

Figure 4. Absolute net doping of JLFET

6. Results and discussion

JLFET devices achieve full depletion by regulating the work function of the gate material in the OFF state. In contrast, in the ON state, they require high doping levels to achieve a substantial drive current. **Figure 5** illustrates the I_D-V_{GS} characteristics of the cylindrical gate-all-around JLFET. These transfer characteristics have been plotted at V_{DS} = 0.01 V, spanning a range of V_{GS} from –0.4 to 1.2 V. The threshold voltage for this particular device has been observed to be V_{th} = 0.37356 V, a suitable value for low-power applications, thanks to the use of a P^+ Poly-silicon gate. **Figure 6** presents the output characteristics of the cylindrical gate-all-around JLFET at various V_{GS} values, specifically 0.8 V, 1.0 V, and 1.2 V, while V_{DS} ranges from 0 to 1 V. This device demonstrates a high ON-state current and a low OFF-state current, showcasing excellent electrostatic control, with a maximum drain current of 2.95×10^{-5} A and saturation slope is about to 3.186×10^{-6} A.

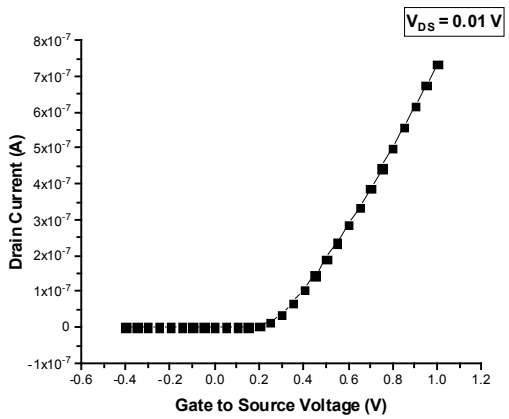

Figure 5. Transfer characteristics of JLFET.

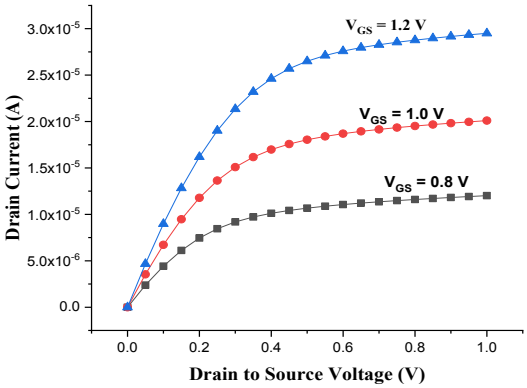

Figure 6. Output characteristics of JLFET.

Furthermore, our designed gate-all-around JLFET boasts a subthreshold swing (SS) of 73.25 mV/dec, which is quite close to the ideal value of 60 mV/dec. The extracted Drain-Induced Barrier Lowering (DIBL) value of 70.9 mV/V underscores its superior resilience against Short Channel Effects (SCEs). **Figure 7** illustrates the transconductance profile of these gate-all-around structures, with simulation results showing a peak transconductance (gm) value of 6.5×10^{-5} Siemens. The transconductance is defined as the derivative of the drain current with respect to the gate voltage, and can be expressed as the ratio of the gate capacitance to the carrier transit time τ, so that $G = 1/2\pi f\tau$. Transconductance is the ratio of drain current (I_D) to gate-source voltage (V_{GS}) when a constant drain-source voltage is applied. The current to voltage ratio is commonly referred to as gain. Transconductance is a critical parameter strictly connected with the threshold voltage (V_{TH}) of MOSETs and both are related to the size of the gate channel.

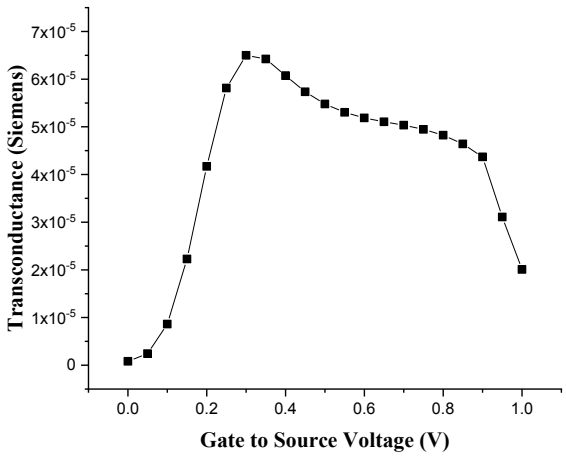

Figure 7. Transconductance of JLFET.

For semiconductor devices, transconductance or Figure of Merit is a crucial parameter. **Figure 8** shows that the transconductance (gm) value possesses quite a close association with low power performance. The simulation results show the value of gm approximated 3803 µS/µm in **Figure 8**.

Moreover, gate all around JLFET possesses the best subthreshold swing (SS) of 73.25 mV/dec, near the ideal 60 mV/dec value. The extracted DIBL value of 70.9 mV/V, reveals the best immunity against SCEs. For the calculation of DIBL, two different threshold voltages have been found, in the first case V_{DS} ranges from 0 to 0.05 V and in the other case V_{DS} ranges from 0.05 to 1 V. **Figure 9** shows the transfer characteristics for execution of DIBL.

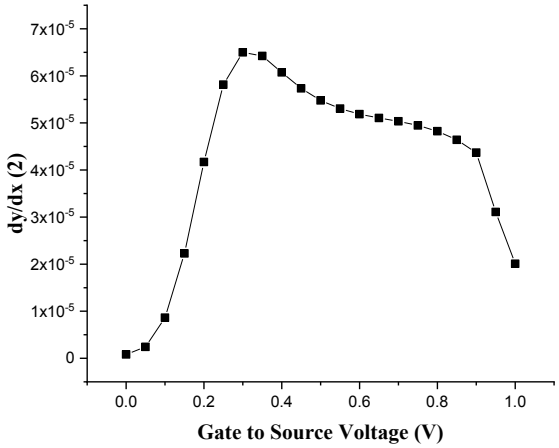

Figure 8. Transconductance of JLFET.

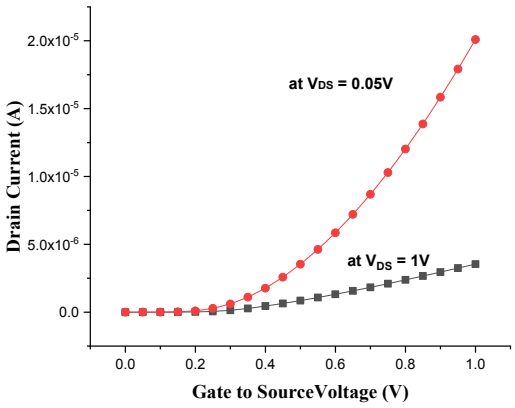

Figure 9. DIBL analysis of JLFET.

7. Comparative analysis

In this paper, the study of JLFET has been provided with its dc analysis. **Table 3** is furnished with gate length, subthreshold swing and DIBL of the proposed structures for comparison. Finally, we conducted a performance comparison of our device with those available in the literature. The smaller SS exhibited by our simulated JLFET holds the potential for low-power operation by reducing the transistor's OFF current. The lowest DIBL and SS values demonstrated by our designed JLFETs underscore their heightened immunity against short channel effects. Subthreshold slope can be defined as the slope of gate voltage to log of the drain current. It is

Table 3. Performance comparison of the our JLFET with other MOSFET structures.

Device Architectures	L_g (nm)	SS (mV/dec)	DIBL (mV/V)	I_{on} (μA)	I_{off} (μA)	I_{on}/I_{off}
Cylindrical Gate-all-around JLFET (This work)	30	73.25	70.9015	20	$3.05421e^{-4}$	65800
GAA JLFET with Stack oxide [15]	25	90.4	112.7	-	-	-
DMG GAA J LFET [15]	25	83.0	70.6	-	-	-
Inversion mode devices [16]	10	83.8	153	-	-	-
Junctionless FinFET PMOS [17]	40	90	-	15.4	-	10^5
Junctionless FinFET NMOS [17]	40	92	-	52.3	-	10^7
FinFET with different dielectric [18]	30		119			
Bulk-FinFET [19]	30	87	107.8	150.24	$5.113e^{-3}$	

an important parameter to analyze the device to be switch on. The smaller values of SS will lead faster the device being ON. The results have shown a good agreement of the values of SS and DIBL for the proposed work. Researchers are focusing on new architectures to obtain the lower value of DIBL as much as possible.

8. Conclusions

In summary, our study encompassed a comprehensive examination and performance assessment of JLFETs in comparison to Conventional Transistors (CTs), particularly in the realm of low-power applications. We scrutinized various performance parameters for JLFETs, encompassing SS, DIBL, transconductance, output conductance, and I_{on}/I_{off}. Our analysis yielded noteworthy results, with JLFETs showcasing impressive attributes such as a minimal DIBL of 70.9 mV and a subthreshold swing (SS) of 73.25 mV/dec. These findings underscore JLFETs' heightened resistance to Short Channel Effects (SCEs) compared to CTs, along with their exceptional current-driving capabilities, positioning them as an enticing choice for advanced semiconductor applications.

Future research explains the use of non-silicon materials with respect to silicon materials like polysilicon, germanium, GaAs and indium-tin-oxide for better results. In the current work, the effects of Short Channel Effects are extensively investigated. The scaling issues were discovered initially followed by the advantage of moving to the 16 nm and 22 nm node technology from 180 nm node transistors. The advantage of introducing 10 nm JLFET is that it results in decrement of size of the transistors, such that more transistors can be implemented on the circuit on a small area. Power consumption is decreased in the circuit. The limitations provided by reducing the size of the transistor i.e. by scaling are short channel effects that are DIBL, Punch through, velocity saturation etc. The present work was sustained with examples in digital field. The digital examples include the implementation of inverter, NOR and NAND on less than 10 nm node.

9. Future scope

For futuristic scope, the focus will be on the usage of high k materials. Research shows mobility degradation due to Poly-Si and Gate Dielectric. A very important effect of thin gate insulation and the

proximity of gate electrode (Poly-Si) is mobility degradation. This affects the ease of carrier transport in the channel. For gate oxide thickness below 1.3 nm is effect becomes a significant challenge. Due to the usage of high-K Dielectrics the channel mobility is significantly reduced as compared to their corresponding SiO_2 devices. There are below given major reasons of this degradation in mobility: (a) Interface traps and oxide charges in the dielectric layer cause Remote Coulomb Scattering which depletes mobility in channel. (b) The formation of soft optical phonons in Hf-based dielectrics may also contribute to mobility degradation. (c) Underestimation of mobility due to various sources of errors in mobility extraction such as over counting of inversion layer charge due to high density of interface traps, high gate leakage can result in underestimation of mobility due to high leakage loss, or error due to contact resistance etc.

Both these effects can be dealt with by replacing the Poly-Si gate electrode with metal electrode. However, reliability challenges with high-K MOSFETs should be a challenge for VLSI engineers. The reliability issues of high-k gate dielectric stacks are caused by several phenomenon's critical causes which are interface layer as well as the dielectric layer. The phenomenon of hot electron aging and Time Dependent Dielectric Breakdown do not pose a major concern while charge trapping presents a very critical reliability issue such as threshold voltage instability. Some other issues that need urgent attention are plasma induced damages and defect study at the interface layer. High-K dielectrics require a careful optimization of the process to minimize the fixed charges.

Author Contributions

All authors contributed to the study conception and design. Data generation, collection and analysis were performed by [Pooja Srivastava]. The first draft of the manuscript was written by [Pooja Srivastava], [Aditi Upadhyaya], [Shekhar Yadav] and [C.M.S. Negi], commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Conflict of Interest

There is no conflict of interest.

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